

**ALL-COPPER CHIP-TO-SUBSTRATE INTERCONNECTS FOR
HIGH PERFORMANCE INTEGRATED CIRCUIT DEVICES**

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Chemical and Biomolecular Engineering

Georgia Institute of Technology
May 2009

ALL-COPPER CHIP-TO-SUBSTRATE INTERCONNECTS FOR HIGH PERFORMANCE INTEGRATED CIRCUIT DEVICES

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In dedication to my loving wife Jessica and my two sons Jackson and Alexander

ACKNOWLEDGEMENTS

I would first like to thank my advisor, Dr. Paul Kohl, for all of the direction and discussions that allowed me to succeed here at Georgia Tech. He has helped me to develop into a researcher that I could not have become otherwise. I would also like to give a special thanks to Dr. Sue Ann Bidstrup Allen, Dr. Dennis Hess, Dr. Thomas Fuller, Dr. James Meindl, and Dr. Peter Hesketh for participating in my thesis committee. They have all provided helpful input at different points in my work. I would like to give a very special thank you to Daphne Perry for her support and consistent help with all of my needs for the lab and travel throughout my time here. Also, thanks very much to the SRC for funding this project and providing such a well designed program to develop young graduate engineers for future professional employment.

The Kohl research group is a close-knit team of chemists and chemical engineers and I know that my work would not have been a success without all of their support with experiments, data analysis, and many research related discussions. Thanks are especially due to Ate He for his guidance in the start of my project. Thank you also to C. Hunter Lightsey, Venmathy Rajarathinam, SeongHo Park, and William E. Mustain for all of their efforts to provide ideas, advice, and opinions related to this work.

Thank you to my wonderful parents Kenneth and Wynona Osborn, without them I would never have even dreamed of making it to this point. Finally and most importantly I would like to thank my wife for being unbelievably supportive through all these years of undergraduate and graduate school. She has always inspired me to do great things.

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LIST OF SYMBOLS

μm	Micrometer
μN	Micronewtons
A	Amperes (electrical current)
A(hc)	Contact Area Function
Ag	Silver
Ar	Argon
Au	Gold
Cr	Chromium
Cu	Copper
dB	decibel
Er	Reduced Elastic Modulus
eV	Electron Volt
H	Hardness
hc	Contact Depth
kgf	kilogram force
mm	Millimeter
nm	Nanometer
Pb	Lead
Pd	Palladium
Pmax	Load max
ppm	Parts per Million
S	Stiffness

Si	Silicon
SiO ₂	Silicon Dioxide
Sn	Tin
Ti	Titanium
W	Watts
γ	Poisson's Ratio

LIST OF ABBREVIATIONS

AES	Auger Electron Spectroscopy
BGA	Ball Grid Array
BT	Bismaleimide Triazine
CHCO	Formaldehyde
CMOS	Complimentary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
COB	Chip-on-Board
CSP	Chip-scale Package
CTE	Coefficient of Thermal Expansion
DC	Direct Current
EDS	Energy-Dispersive X-Ray Spectroscopy
EDTA	Ethylenediaminetetraacetic acid
FR-4	Fire Resistant 4 (Printed Circuit Board)
GHz	Gigahertz
GHz	Gigahertz
GPa	Gigapascal
GPD	Generalized Plane Deformation
I/O	Input/Output Connections
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MPU	Microprocessor Unit
NiB	Nickel Borate

PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PEG	Polyethylene Glycol
RPM	Revolutions per Minute
SEM	Scanning Electron Microscope
SoC	System on a Chip
SoL	Sea of Leads
SPS	Sulfopropyl Sulfonate
TEM	Transmission Electron Microscope

SUMMARY

In this work, all-copper connections between silicon microchips and substrates are developed. The semiconductor industry advances the transistor density on a microchip based on the roadmap set by Moore's Law. Communicating with a microprocessor which has nearly one billion transistors is a daunting challenge. Interconnects from the chip to the system (i.e. memory, graphics, drives, power supply) are rapidly growing in number and becoming a serious concern. Specifically, the solder ball connections that are formed between the chip itself and the package are challenging to make and still have acceptable electrical and mechanical performance. These connections are being required to increase in number, increase in power current density, and increase in off-chip operating frequency. Many of the challenges with using solder connections are limiting these areas. In order to advance beyond the limitations of solder for electrical and mechanical performance, a novel approach to creating all-copper connections from the chip-to-substrate has been developed. The development included characterizing the electroless plating and annealing process used to create the connections, designing these connections to be compatible with the stress requirements for fragile low-k devices, and finally by improving the plating/annealing process to become process time competitive with solder. This work resulted in many significant conclusions about the mechanism for bonding in the all-copper process and the significance of materials and geometry on the mechanical design for these connections.

The all-copper process entails electroless copper deposition between two copper pillars, followed by low temperature annealing to 'knit' together the seam left between

the two pillars and mechanically strengthen the joint. It was found that using a commercially available electroless copper bath for the plating, followed by annealing at 180 C for 1 hour, the shear strength of the copper-copper bond was approximately 165 MPa. Cross-section analysis showed that during the deposition process plating occurs until a fine seam remains between the two plated surfaces. Then, upon annealing the seam begins to diminish and finally disappear after annealing at 180 C. This is significant since 180 C is compatible with cost-effective organic substrate materials such as FR-4, which are commonly used for typical flip-chip packaging. The process was also characterized to have excellent capabilities related misalignment tolerance. The all-copper bonds formed with planar misalignment greater than the pillar diameter. In addition, height mismatches of 65 μm were also successfully bonded.

The mechanical modeling and design for the copper pillar connections showed that if correctly fabricated, the copper connections could satisfy the low stress requirements for devices with fragile low-k on-chip interconnect networks. It was found that the stress placed on the surface of the silicon die was a strong function of both the elastic modulus of the polymer collar surrounding the copper pillar and the cross-sectional shape of the pillar. Using elliptical shaped copper pillars with a specifically tailored elastic modulus polymer collar, stress below the yield for lead-free solder (~45 MPa) could be achieved.

An improved electroless deposition process was developed using elevated temperature and PEG suppression to create non-porous bonded copper-to-copper joints. Using the commercial bath as a basis, 1 ppm PEG was added, and the deposition temperature was raised to 70 C. At these conditions plating time was reduced from 18

hours at room temperature to 2 hours. This translates to a 9X reduction in plating time. After annealing and shear testing it was found that the new plating process succeeded in creating mechanically stable all-copper connections. Cross-sectional analysis confirmed that a seamless copper-to-copper joint was formed after the annealing process.

CHAPTER 1

INTRODUCTION

1.1 Introduction to Microelectronic Packaging

Transistor scaling, shrinking the critical dimensions of the transistor, has led to continuous improvements in system performance and cost. Higher density of the transistors and larger chip size has also led to new challenges for chip-to-substrate connections. The pace of change in packaging and chip-to-substrate connections has accelerated because off-chip issues are increasingly a limiting factor in product cost and performance. Chip-to-substrate connections are challenged on many fronts, including number of signal input-output (I/O) connections, I/O that operate at high-speed, power & ground I/O, and low cost.

Chip-to-substrate interconnects provide power, electrical contacts, and a mechanical link between the chip and the substrate. The two most common chip assembly schemes today, wire bonding and flip chip bonding are illustrated in Figure 1 (a) and (b), respectively. [1-4] The area-array flip-chip configuration provides for a higher number of I/O and the electrical environment is superior to wire bonding because it has lower inductance and capacitance. An area array of flip-chip solder balls has more I/O than peripheral wire bonds. Flip-chip connections also provide an additional thermal path for chip cooling through the I/O.

Flip chip assembly uses metal connections; often solder spheres, to connect the chip to the substrate and/or the substrate to the board as shown in Figure 1 (b). Chips can also be connected directly to the board in a chip-on-board (COB) configuration, Figure 1 (c). COB is a less costly and lower profile (total height) technology; however, the substrate helps in electrical fan-out and allows for a higher number of I/O. The substrate also assists in assembly of a heat-sink which is needed on high power chips.

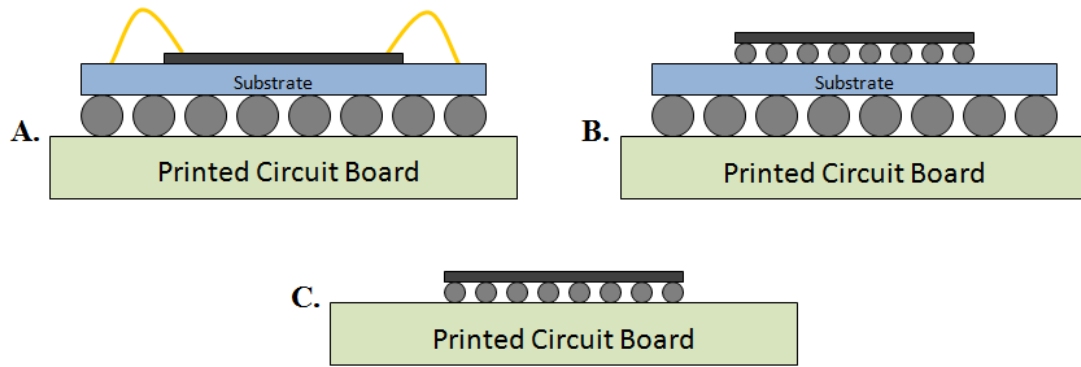


Figure 1.1: Illustration of (a) chip-to-substrate wire bonding, (b) chip-to-substrate flip-chip interconnection, and (c) chip on board flip chip connection.

1.2 ITRS Projections for Flip-Chip Connections

Projections on the number and density of I/O can be made based on transistor scaling, and projections on chip size and performance. Table 1 lists some of the International Technology Roadmap for Semiconductors (ITRS) projections for high performance chips.[5] Although the power consumed in high performance chips has been capped at 198 W, the direct current (DC) will continue to increase because the supply voltage will drop. If the current is to be delivered at the low operating voltage, an increasing number of I/O will be involved so that the threshold for electromigration is not crossed and the power is delivered across the chip, where it is used locally.

The signal I/O will be especially challenged because the number of I/O will increase, reducing the I/O pitch, and their performance must improve so that they can support higher off-chip speed communication. The improvement in I/O design needs to occur with a decreasing cost-basis, as shown for example in the cost per pin number. Not shown in Table 1.1 are the mechanical requirements of future I/O. The dielectric constant of the on-chip insulators is being lowered so as to decrease interconnect delay. This will lead to more fragile on-chip dielectrics which will no longer be able to support the high stress levels imposed by the I/O. Future chip-to-substrate connections will likely

need to be mechanically compliant to compensate for the mechanical stresses induced by the coefficient of thermal expansion (CTE) mismatch between the semiconductor chip and the package substrate or board. Normally, one would expect the I/O induced stress to rise as the size of the solder ball is reduced and the gap between the chip and substrate is lowered. The shrinking size of the flip-chip solder balls is reflected in the pad pitch and pin-count.

The increase in chip-to-substrate speed is extremely important, particularly for processor-to-memory access. The increase in speed is however most challenging because signal degradation and distortion can occur unless the electrical characteristics (resistance, capacitance, inductance, and impedance) are acceptable. Finally, as with most electronic components, performance improvements become commercially viable only when the cost structure facilitates improved performance/cost. Thus, the higher performance I/O must be achieved at a lower per unit cost.

Table 1.1 Select ITRS values for high performance chips.

Year	2005	2007	2010	2013	2016	2020
MPU Current, A	172	172	198	220	248	283
MPU Power, W	167	198	198	198	198	198
Chip-to-Board Speed, GHz	3.1	4.9	9.5	18.6	34.9	72.4
Pad Pitch, flip-chip, μm	150	130	120	110	95	85
Package Pin-count	3400	4000	4851	5616	6501	7902
Package Cost per pin, cents	1.78	1.83	1.56	1.34	1.15	0.94

1.3 Research Objectives

Solder has many weaknesses in flip-chip applications and faces ever greater problems as the size and pitch of the solder balls shrink with device scaling. The International Technology Roadmap for Semiconductors forecasts minimum pitch for area-array connections to shrink to 120 μm , 100 μm , and 85 μm , in 2010, 2015, and 2020, respectively.[5] The small stand-off height accompanying fine-pitch solder balls exacerbates the problems associated with underfill materials in small gaps, which are needed with solder. Solder forms brittle copper-tin intermetallics during reflow that can compromise its thermo-mechanical reliability. Solder also has low electromigration resistance which is becoming more important as the diameter of the flip-chip connections shrink and DC power requirements increase. High aspect ratio flip-chip connections are needed for high input/output (I/O) density. Copper pillars capped with solder domes are increasingly used to increase the stand-off height at the first-level of packaging. Copper pillars on both the chip and substrate also move the location of the brittle copper-tin intermetallics away from the high stress region where the copper pillar (or solder ball) intersects the chip or substrate.

All-copper connections from chip-to-substrate eliminate many of the issues with solder, underfill, and the intermetallics formed between tin and copper. Copper has superior electrical conductivity and electromigration resistance versus solder. It also has superior mechanical properties, such as yield stress and Young's modulus. These mechanical values, along with the ability to fabricate high aspect ratio connections, can be used to form mechanically compliant interconnect structures. The elimination of underfill will improve the signal I/O environment by lowering the permittivity and loss of the I/O. This will become increasingly important with time as the off-chip frequency

continues to rise.[5] Having no tin based materials present eliminates brittle intermetallics which will improve the thermo-mechanical reliability of the device. Finally, high aspect ratio copper connections can be fabricated with very fine pitch without compromising minimum stand-off distances between the chip and substrate. The elimination of solder, the under-bump metallurgy needed for solder, flux, underfill, and stripping chemicals could reduce costs and environmental impact.

The scope of this work was to develop a process that yields all-copper connections from the chip to the package substrate. The all-copper process must respect the needs for packaging in terms of cost and manufacturability. Typical packaging houses do not use cost prohibitive on-chip processing techniques such as any process requiring a vacuum (i.e. plasma deposition, plasma etching, sputtering). In addition the process must be competitive or better than solder in all areas that solder excels. These are primarily related to misalignment tolerance, and low temperature processing. Packaging with cost-effective organic printed circuit boards requires that elevated temperature excursions be as low as possible, but definitely below 250 C. The final goal of this work was to design copper pillar connections so as to be compliant and reliable without the need for underfill materials. This will eliminate the need for underfill materials and processing, possibly saving costs and at the same time increasing the possible I/O density without worry for underfill flow.

CHAPTER 2

REVIEW OF FUTURE HIGH-PERFORMANCE PACKAGING SOLUTIONS

2.1 Compliant Solder-based I/O Structures

The need for small chip footprint, especially in portable electronics, and higher I/O density has created the need for new packaging technologies. Chip-scale packages were created to address a rapidly growing segment of the market. These chip-scale packages enabled a high silicon packing density, however, CTE mismatch between the silicon and the board needed to be addressed.[6,7]

2.1.1 Peripheral-to-flip-chip Area Array Structures

Reducing the package footprint has been an important contributor to reducing the overall system size, weight, and cost. However, reducing the total package size lowers the area over which the mechanical strain is distributed. Numerous approaches have been taken to address the need for mechanical compliance in low-cost, small footprint packages. Some of the first compliant flip-chip structures used flip-chip attachment to convert peripheral I/O into an area array so as to shirk the footprint of the die. Pre-fabricated film or tape-based chip-to-substrate I/O has been used to connect the chip to printed wiring boards. Amkor and Toshiba have used this style of interposer.[6,7] The interposer (tape) is applied to the die followed by assembly. The chip can be wire bonded to the interposer followed by flip-chip attachment of the interposer-plus-chip to the printed wiring board.

A degree of compliance is given to the interposer and can be enhanced by using 3-dimensional, spring-like structures. Tessera has developed a compliant vertical link

technology where the metal interconnection in the interposer lifts off the flexible foil by the injection of an encapsulant between the interposer and the IC.[8] Figure 2.1 shows the Tessera BGA for perimeter I/O. The device is then attached to the board by use of solder balls. The Tessera BGA provides redistribution from the perimeter I/O to area array so that the pitch on the board can be eased to coarser values. The flexible spring-like structures can bend and relieve the stress generated by the CTE mismatch between the chip and the substrate.

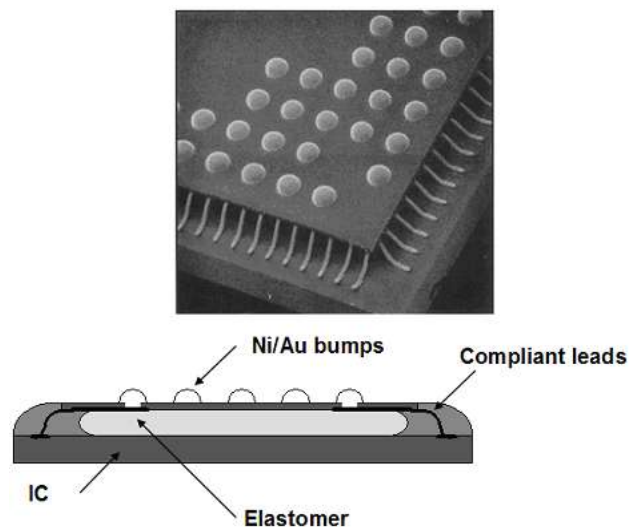


Figure 2.1: Picture and cross section of micro BGA from Tessera

2.1.2 Redistribution Using Area Array Solder I/O

Redistribution of the I/O on a chip to a more convenient form can be accomplished in many ways. Redistribution can more equally distribute the I/O across a chip and can be used to build mechanical compliance into the I/O. The redistribution can be accomplished by adding an interposer layer. The interposer can be introduced through the use of a prefabricated layer or by fabricating the layer directly on the chip in wafer form. The wafer-scale interposer layer requires that one performs extra processing steps after the chip back-end processes are complete. An example of a prefabricated interposer

structure is shown in Figure 2.2 which shows the WAVE package for area array I/O devices. An interposer containing the flexible link is attached to the chip I/O. The solder ball is used to attach the chip to the substrate.

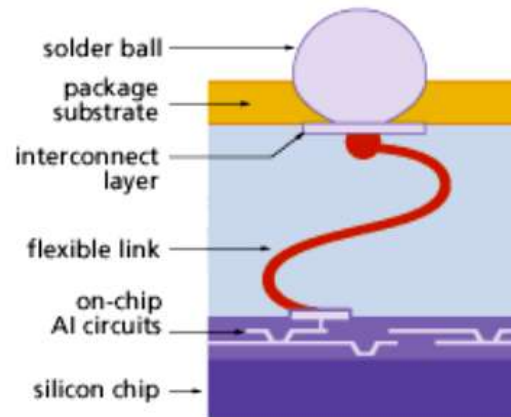


Figure 2.2: WAVE technology developed by Tessera

2.1.3 Wafer-Scale Compliant I/O

Compliant, solder-based I/O can be fabricated in wafer form after normal back-end chip interconnect is complete. After normal chip fabrication, a final polymer-metal build-up process can be used to redistribute the I/O. Once the wafer level package is complete, the chips are separated and assembled. The first uses were in lower pin-count devices and were driven by cost reductions. Since a traditional package is not required and the size of the printed wiring board can be reduced (smaller IC footprint), the packaging costs are lower. The mechanical requirements are modest since the chips are small, and the number of I/O is low.

A small amount of compliance between the chip and substrate was achieved by Fujitsu in the SuperCSP package.[7] Short copper posts were fabricated on the chip in wafer form. A polymer was then used to encapsulate the posts. The structure has a degree of compliance because the post can elastically deform and the polymer encapsulation can help distribute the stress. Most of the compliance was provided by conventional solder

bumps attached to ends of the posts. The Fujitsu SuperCSP used copper-posts 350 μm diameter and 100 μm tall. Special equipment has been developed to injection mold a polymer encapsulant around the posts followed by solder ball attachment. Oki and Casio have developed a similar structure for use in low pin count devices.[7] Ibiden has developed a thin, flexible post in the second layer of polymer used in the redistribution build-up. These 'post' technologies show the importance of in-plane (x-y direction) compliance in producing a reliable, wafer-level packaged device. The solder joint on the copper post provides an inexpensive way to compensate for any z-axis (height) mismatched between the chip and substrate. The solder ball can be slightly compressed or elongated during reflow to make up for non-planarity in the parts. Intel Corporation also uses copper posts with an attached solder ball to package microprocessors.[9] The short copper post also lifts the brittle solder joint off the chip surface to improve reliability. The highest stress point of the flip-chip solder joint is the intersection of the I/O and the chip surface.

Chip-to-substrate structures with higher I/O density and much greater compliance have been developed. A Sea of Leads (SoL) technology was developed as an enabling technology for future chip-to-module interconnections.[10,11] SoL wafer level packaging technology provides an ultra-high I/O density of x-y-z compliant leads ($>10^4$ per cm^2) and can enhance the performance of a system on a chip (SoC) by routing critical on-chip global interconnects off-chip to reduce signal delay and thus increasing global clock frequency.[10,11] The addition of an embedded air gaps into SoL adds vertical compliance (z-axis) needed for wafer level testing and mating to non-planar boards. Air-gaps also serve to lower the dielectric constant of the interconnect. Figure 2.3 shows a cross-section of process flow for an x-y-z compliant lead.[12]

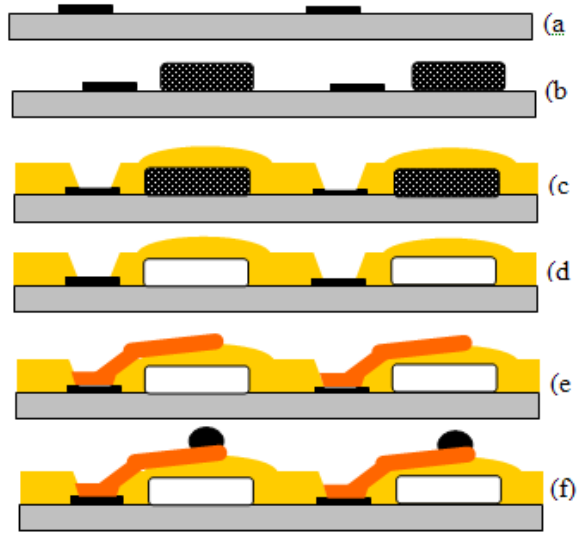


Figure 2.3: Build-up process of embedded air-gaps.

The exposed I/Os are shown in Figure 2.3a. A sacrificial material shown in Figure 2.3b is overcoated by a flexible material and vias are opened to the bond pad in Figure 2.3c. When the overcoat elastomer is curing in Figure 2.3d, the sacrificial material decomposes leaving a buried air-cavity. The exact compliance of the final structure depends on the size and shape of the air-cavity, and the elastic properties of the overcoat material. In-plane compliance (x-y compliance) was obtained by releasing the metal lines off the polymer surface. The deflection was measured to be greater than 30 μm . While the leads are x-y-z axis compliant, they are short in length and thus exhibit minimal parasitics from DC to 45 GHz. The calculated resistance and inductance of the leads are less than 25 m Ω and 0.1 nH, respectively. Low electrical parasitics are desirable at both low and high frequencies for efficient conductive coupling of power, low power dissipation in the leads and thus low heat generation by the package. The microwave characteristics of SoL were measured at wafer-level using a two-port network analyzer with 150 μm coplanar ground-signal-ground (GSG) probes. To characterize the

compliant interconnects, 15 μm thick Au leads were fabricated on a 15 μm thick polymer film. The return-loss and insertion-loss of the GSG lead interconnection were measured to be less than 20 dB and 0.2 dB, respectively, at 45 GHz.[13] In comparison, the insertion losses before and after the addition of underfill within a flip-chip package mounted on an alumina substrate with 75 μm wide x 150 μm height bumps interconnected by 600 μm long 50 Ω coplanar waveguides were found to be 0.6 dB and 1.8 dB, respectively, at 40 GHz.[12,13]

A variety of complex, three-dimensional structures have been produced by using standard lithography and metal deposition.[14-19] Figure 2.4 shows a one-turn helix structure produced by standard metallization and photolithographic techniques. The dimensions of the helix can be varied over wide ranges. The radius of the beam is critical to the compliance and electrical properties of the interconnect.

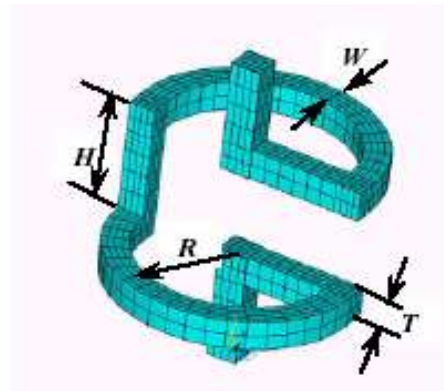


Figure 2.4: Structure of a G-helix

The structure has been simplified to eliminate one of the half-turn structures, shown in Fig. 2.4.[17] The electrical properties of the compliant I/O are an essential element of the design. Of particular interest for helix structures is the self-inductance, which ranged from 0.03 to 0.15 nH for the designs studied.[17]

A bimetallic beam structure has been designed and studied.[18] The bimetallic internal stress gradient in the beam creates an upward bending of the beam upon release from the surface. Solder attachment metal on the released end of the beam provides for attachment to the next layer of packaging.

Finally, more complex beam shapes have been investigated. Liao et al. have studied released beams on the chip.[19] The beams are anchored on both ends (on the chip) and released in the middle. The released portion of the beam can take a variety of forms, including ‘S’ shaped elements. A solder attachment bump can be placed in the middle of the release beam. This provides extensive design freedom.

2.2 Improved Mechanical Performance Solder Capped Structures

A current modification to solder type flip-chip connections that has received significant attention for research and development is the solder capped structure. Moving the more fragile solder material off the chip and/or package surface and instead placing a tougher material such as a copper bump or pillar underneath the solder connection creates a more thermo-mechanically reliable structure. Since the highest stress during thermal loading is now experienced in the higher yield stress material, the number of cycles to failure can potentially be significantly increased. Additionally, since the aspect ratio of the connection is no longer directly related to the diameter of the solder ball, finer pitch connections can be made at more practical stand-off distances. Increased allowable separation between chip and substrate is important for both increasing reliability of the connection itself and allowing for underfill to be more easily flowed in between the chip and substrate.

Several researchers have pursued structures such as the copper pillar with solder cap.[20-22] This structure, as demonstrated in Figure 2.5, has both merits and problems. Copper has excellent properties for interconnects such as low electrical resistance, high allowable current density, and yield stress. However, typical tin based solders capping

these structures lead to brittle intermetallics. Therefore, underfill is still necessary to ensure thermo-mechanical reliability. The use of copper bumps for this application has promise as an interim solution until an effective solder-free solution can be developed. The true capability of the pillar interconnect cannot be realized with the solder cap since it will still be limited both electrically and mechanically by the properties of the solder portion. Other metals such as nickel have also been demonstrated for the solder-capped pillar approach.[23] The materials available to create capped solid metal pillar connections are highly variable and most likely depend on cost and application requirements. Both leaded and lead-free solders have been used, in addition to other less common solders such as tin-gold. Choosing what type of solder is again most likely dictated by needs for specific applications such as allowable reflow temperatures and the solder deposition method.

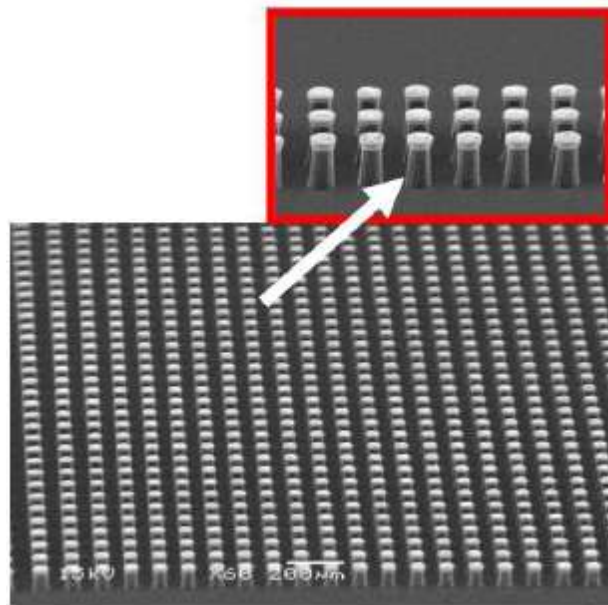


Figure 2.5: High aspect ratio copper pillars capped with solder

Other work has been pursued to attempt to make the mechanically rigid, high yield stress, solid metal pillar more compliant.[24] By applying a metal conductor to the

exterior of a polymer pillar, the compliance of the interconnect structure could be improved. Aggarwal et al. showed that by using a compliant polyimide core material with a copper shell the compliance increased versus the use of a solid copper pillar of the same diameter (as shown in Figure 2.6).[24] Due to the skin effect at high operating frequency, the copper shell does not have to be very thick since the signal does not penetrate deep into the metal. For example, copper has a skin depth of approximately 1.2 μm at 3 GHz operating frequency. This portion of metal is primarily involved in the transmission of the electrical signal. As operating frequency increases the skin depth continues to decrease which works in favor of these structures since the exterior copper thickness limits the mechanical compliance.

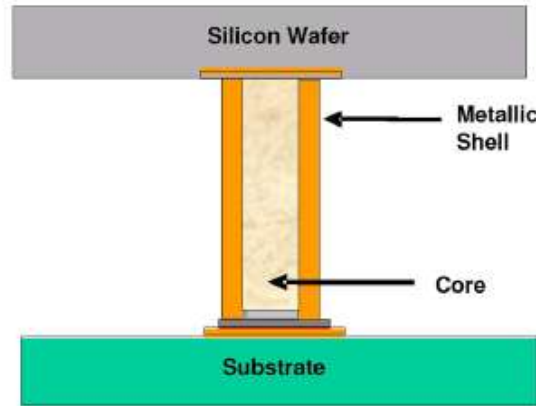


Figure 2.6: Metal-clad polymer pillar with solder cap to improve compliance

Another alternative to creating the solder bond at the end of the interconnect structure is to place the solder between two bumps or pillars. By removing the solder connection from both the chip and substrate surfaces, the highest stresses in the structure are entirely experienced in the high yield stress, higher elastic modulus material of the bump and not the more fragile solder or brittle intermetallics. It is well known that tin

and copper form predominantly two intermetallics materials: Cu_3Sn and Cu_5Sn_6 that are brittle and have poor mechanical reliability.

Huffman et al. have shown that pure tin placed between two copper bumps can be used to create a solid pillar interconnect (as shown in Figure 2.7). [25] It was shown that 2 μm thick tin layers would form homogeneous Cu_3Sn intermetallics in the bonded region, but were very sensitive to non-planarity between chip and substrate. Small variations in the vertical separation between bumps could prevent forming of a solid bond. Thicker tin layers, 3.7 – 6 μm , were used to alleviate the sensitivity to non-planarity and lower bonding pressures were used to prevent squeeze out of the tin. Unfortunately, this resulted in bond intermetallics layers consisting of a tri-layer structure of $\text{Cu}_3\text{Sn}/\text{Cu}_6\text{Sn}_5/\text{Cu}_3\text{Sn}$. Higher pressures could still achieve the homogeneous Cu_3Sn intermetallic but led to significant squeeze out of tin. The results also showed that, based on die shear testing, the homogeneous bonded Cu_3Sn intermetallic led to higher shear strength. Overall the process was found to be highly sensitive to non-planarity between chip and substrate which would not be practical for production assembly since organic boards are not uniformly planar with respect to a silicon die. Iwasaki et al. have also demonstrated a technique for bonding between two bump structures that also shows need for highly planar surfaces. [26] These techniques that require such strict planarity between bonding surfaces will mostly be restricted to bonding between silicon die for applications such as 3-D integration.

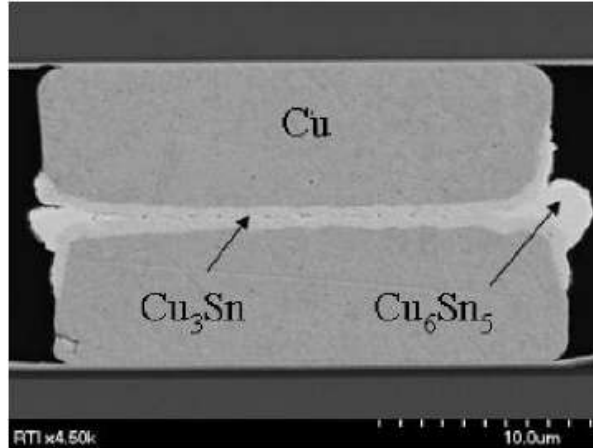


Figure 2.7: Tin bonded between two copper bumps

2.3 Solder-Free Chip-to-Substrate Interconnects

Current industry standard flip-chip interconnects employ the use of solder balls to make electrical connection between the chip and substrate. Solder has many weaknesses for this application, and they are becoming more important as the required interconnect size continues to shrink to meet the I/O demands of modern high performance microchips. The ITRS forecasts minimum pitch for area array interconnects to shrink to 120 μm , 100 μm , and 85 μm , in 2010, 2015, and 2020 respectively.[5] Such fine pitch interconnect needs are challenging for manufacturability and reliability. Since the solder connections are formed with roughly spherical solder balls, the stand-off height between chip and substrate is limited to approximately the solder ball diameter. Therefore, as pitch decreases the gap between the two surfaces will continue to shrink. The challenges related to this loss in separation are focused into two areas: underfill and thermo-mechanical stress. During the packaging process underfilling between the chip and substrate is done with a silica particle filled epoxy material to alleviate thermal stress/strain on the weak solder connections. Flowing underfill between the surfaces is becoming more and more of a challenge as the distance between the two surfaces continues to shrink.[27] Since thermo-mechanical strain is generated between chip and

substrate during operation due to CTE mismatch between Si and FR-4, chip-to-substrate interconnects must withstand this stress. As the chip stand-off distance becomes shorter, creating reliable solder connections is very challenging.

Solder has limitations in many areas including the formation of brittle intermetallics with copper that can compromise thermo-mechanical reliability. Solder also has low electromigration resistance which is becoming more important as the diameter of interconnects continue to shrink and power requirements increase. Solder has a limited allowable range of current density due to this poor electromigration resistance. Therefore, alternative interconnect strategies are being explored that do not require solder. By removing the tin based material, the electromigration resistance and therefore the allowable current density for interconnects will increase. For example, by creating the connection between chip and substrate entirely with metallic pure copper, the allowable current density increases by approximately 10 times.

Despite the properties that make solder undesirable for future I/O needs, solder still has properties that are very useful for manufacturing. Primarily solder has exceptional capabilities for low temperature processing that is compatible with the low cost organic substrates such as FR-4. Solder also can elongate and flatten during reflow to bond misaligned and non-planar locations between chip and substrate. These properties simplify manufacturing and increase yield, and therefore any practical solution for future interconnect needs should attempt to satisfy these properties that have made solder connections tractable for so many years.

Solder-free solutions which satisfy the need for higher density and improved reliability interconnects at this level will be discussed in the following sections. Several different solutions have been active topics of research. Electrically connecting the chip to the substrate without the use of low temperature melting solder materials is a very challenging problem.

2.3.1 Copper Interconnects

One of the most attractive solder-free solutions is to incorporate only copper into the interconnect structure. This would potentially allow for copper electrical connections made directly from the lowest interconnection level on-chip all the way through the package and printer wiring board. Elimination of any additional metals or other conductive materials would improve reflection loss, impedance mismatch, and generation of inter-metallic compounds. The low resistivity, high electromigration resistance, and low cost of copper make it an attractive solution for all electrical connections. The performance of such an interconnect scheme would help to minimize RC delay for the entire system. Additionally, since copper has much higher yield stress and elastic modulus versus typical tin based solders, mechanically reliable chip-to-substrate connections can be designed. Several methods have been developed and proposed to bond copper for this application. Research into copper bonding for chip-to-substrate interconnects is actively being pursued and no single solution has emerged as the definitive technique. Several of the methods for making copper connections will be discussed.

2.3.1.1 Copper Wafer Bonding

One of the first techniques developed to create a solid copper-to-copper connection between chip and external circuits was reported by Chen et al.[28] In this process pressure and temperature are applied to encourage metallic bonding to occur between two distinct copper surfaces. Typically two wafers coated with evaporated copper and tantalum diffusion barrier are placed facing one another. Then, the stack is annealed at temperatures typically in the range from 300°C to 450°C. During the anneal process pressure, typically in the range of 4000 mBar, is applied to bring the two surfaces into intimate contact across the entire wafer surface and promote bonding.

Under TEM analysis, the process exhibits excellent bond quality between the two evaporated copper films.[29,30] As can be seen in Figure 2.8, the two copper surfaces readily bond and form a single copper layer at a bonding temperature of 400°C followed by anneal at 400°C in a nitrogen environment. It has been shown that without sufficient post-bonding anneal in a nitrogen environment the bond is not stable and is easily broken.[31] Therefore, the optimum conditions for bonding were found to reside in the range of 400°C for 30 minutes followed by anneal also at 400°C for 30 minutes or 350°C for 30 minutes followed by annealing at 350°C for 60 minutes. Both bonding process conditions were demonstrated to generate excellent bonding between the copper films.

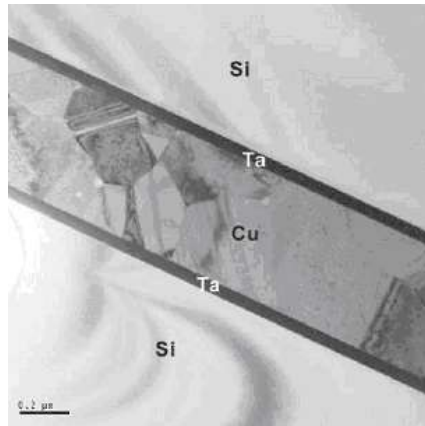


Figure 2.8: TEM of copper wafer bonding process using 400°C bonding and annealing temperature

To analyze the strength of the bond between the copper surfaces qualitative and quantitative approaches were taken. First, the bonded wafers were subjected to dicing after bonding. Here the post copper bonded wafer pair was cut under a dicing saw which induces stress into the bond. Experiments showed that bonding above 350°C was sufficient for all diced specimens to survive. After dicing, individual specimens were subjected to another qualitative test, the tape test. Here 3M Scotch tape was adhered to one of the silicon pieces. By pulling on the tape either the copper to copper bond would

fail and the die separate or the tape would be removed from the backside of the die. Again, high temperature annealing, $>300^{\circ}\text{C}$, led to high number of successful tests without failure.

Something of interest discovered from these tests is that it appears annealing the structure in a nitrogen environment only enhances bonding for samples bonded at 300°C or greater. Below 300°C as the bonding temperature decreases, annealing after bonding appears to significantly degrade the bond and therefore greatly increase the number of failures in both the dicing and tape tests. This result is proposed to be the result of the thermal stress on the copper bond during the nitrogen anneal step.[31]

Further quantitative testing of the process via both a normal direction pull test and shear testing confirmed that temperatures above 300°C allow for sufficient thermal activation to generate an effective bond between the copper layers. The pull test showed bond strength as high as $\sim 70\text{ MPa}$ for samples bonded and annealed at 400°C . Shear tests further confirmed that significantly improved bonding occurs in samples bonded and annealed at 400°C .[32]

Copper wafer bonding shows excellent promise towards generating continuous copper connections between silicon and silicon [33], or possibly silicon and ceramic packages, but it will not be possible to utilize for organic substrate packaging due to the high temperature requirements. While making high quality connections for vertically integrated systems such as stacked silicon die is important for the future, organic substrate based packaging is of much more mainstream importance.

2.3.1.2 Surface Activated Bonding

While copper wafer bonding mentioned above generated excellent bonding between copper surfaces, it does have limitations. One important limitation is that of temperature tolerance. Since current flip-chip type packages utilize organic substrates, such as FR-4, temperature excursions of 400°C are not possible. Typical organic printed

circuit board materials like FR-4 begin to thermally decompose and degrade when held at temperatures exceeding $\sim 250^{\circ}\text{C}$. This decomposition temperature varies for specific organic substrates but 250°C is a good metric. In the Surface Activated Bonding (SAB) technique, developed by Kim et al. at the University of Tokyo, bonding between copper surfaces is realized at room temperature.[34]

Unlike the wafer bonding method, no elevation in temperature is required to merge the two copper surfaces and therefore create the interconnection between chip and substrate. For SAB two copper surfaces are placed into a high vacuum environment, typically in the range of $10^{-5} - 10^{-7}$ Torr. Once under vacuum the surfaces are cleaned via an argon (Ar) ion beam with typical energy in the range of 40 – 100 eV. The Ar ion beam is used to remove surface oxide and any other chemical contamination on the copper. In fact the energy is more than sufficient to sputter the copper surface itself. Therefore, the cleaning in fact removes a small portion of the copper to fully decontaminate the surface. Since the sample is never removed from the UHV environment, there is little if any re-oxidation of the surface that takes place. This fact is verified by Kim et al. by Auger electron spectroscopy (AES) of the copper surfaces before and after the ion beam activation process. Furthermore, the authors comment that bonding is always performed within 60 seconds of the activation process to prevent any effects from residual gases oxidizing the surface.

Once the surfaces are fully cleaned and activated, they are brought into contact and external pressure is applied to force intimate contact across the surface and encourage bonding between the two copper regions. It is critical that the entire process takes place in the vacuum chamber; therefore, the authors developed a custom system that allowed for ion beam cleaning and flip-chip bonding to take place without the need to vent or open the chamber. During bonding the externally applied pressure serves as the only driving force to merge the copper surfaces. Typical applied pressures are in the range of 6 – 15 MPa. There is no temperature elevation during the bonding process.

The fact that temperature is not changed is important for flip-chip bonding for two reasons. First, the low temperature processing allows for no degradation of the organic substrates and continued use of these cost effective materials is possible. Second, Shigetou et al. comment in the more recent work on SAB that maintaining alignment between ultra-fine pitch copper pads would be nearly impossible with elevated temperatures due to the thermal strain. Shigetou et al. demonstrated bonding of “bumpless” copper interconnects of 10 μm pitch with $\pm 1 \mu\text{m}$ accuracy (as shown in Figure 2.9).[35] This fine structure allowed for connecting $\sim 100,000$ I/O which is remarkable.

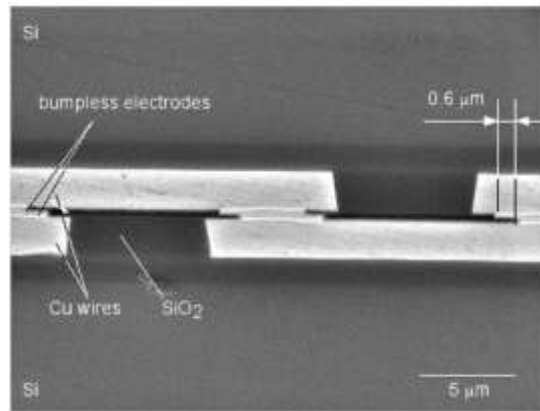


Figure 2.9: Bumpless Interconnects formed via Surface Activated Bonding

TEM analysis confirmed that the two copper regions do in fact merge and exhibit excellent bonding despite having no elevated temperature driving force. Kim et al. proposed that the excellent bonding observed is due to the activation process. Since essentially no oxide or other chemical contamination is present on the copper surfaces they readily bond to one another. Additionally, another critical factor in this technique is that of surface roughness. In the initial work by Kim et al., surface roughness was measured by Atomic Force Microscopy (AFM) before and after the activation process.[34] It was found that the activation process had no effect on surface roughness

and therefore the sputtered copper film maintained surface roughness of approximately 1.8nm. Intimate contact between the copper regions is achieved readily owing to their smooth condition. In the later work of Shigetou et al., the copper surfaces bonded were generated via electroplating and chemical mechanical polishing (CMP).[35] Here, the surfaces were found to have 1.2 nm rms roughness via AFM measurement.[35] Having such smooth surfaces is critical to the SAB process since the copper regions on both chip and substrate must be brought into contact during bonding. Since both silicon wafer and organic boards are not flat, they must be able to withstand sufficient external pressure to be made flat for contact during bonding.

To characterize the quality of bond made during SAB, Kim et al. performed a fully bonded wafer dicing test.[34] Similar to the test mentioned above for copper wafer bonding, two eight inch wafers were bonded via SAB. Then, the bonded pair was diced into 10mm x 10mm sections. Results showed that only a few edge pieces were not sufficiently bonded to survive the dicing saw stresses. Additionally, 10mm x 10mm chips that survived dicing were subjected to normal tensile pull testing to attempt to quantify the bond strength. However, the observations showed that samples failed in other areas and not the copper to copper bonded region. The maximum observed tensile strength was 6.47 MPa but was not indicative of the copper bond strength.

Later, Shigetou et al. demonstrated the capability of the technique for bonding “bumpless” copper interconnects. Here individual copper pads were patterned and bonded with SAB. The method demonstrated bonding and successful electrical testing. To demonstrate the capabilities of the technique to generate off-chip interconnections that satisfy the density of global wiring on-chip, 10 μm pitch was used. At such a fine pitch one of the biggest challenges for the experiments was proper alignment between 3-5 μm diameter copper pads. In fact, from the electrical testing experiments the authors mention that misalignment is most likely the largest contributor to contact resistance being greater than expected for a true bulk copper-like connection. With such fine dimensions, even

misalignment of $\sim 1\text{ }\mu\text{m}$ could lead to large increases in contact resistance for $3\text{ }\mu\text{m}$ connections. Yet, the demonstration of such fine pitch and high performance electrical connections is promising for future needs.

2.3.2 Electroplated Copper Column Arrays

Another method to create metallic bonding without the use of solder is ultrasonic or thermo-sonic bonding. For this method ultrasonic energy and/or thermal energy is incorporated into the desired bond region to locally heat due to friction and generate a solid metallic bond. Gao et al. have shown this method to work for bonding electroplated copper columns with gold caps onto aluminum metallization pads.[36] The gold cap readily bonds to the aluminum pad under thermo-sonic bonding conditions giving a continuous metallic connection without the need for solder materials. While thermo-sonic bonding for gold metal has been used for wire bonding applications, it has not been adopted as a flip-chip type packaging solution. Thermo-sonic bonding of gold has been demonstrated previously using gold stud bumps by others since 1993.[37] However, the gold stud bump approach has not been adopted.

Therefore, Gao et al. developed an alternative structure that utilizes the thermo-sonic bonding capabilities of gold without the need for such a serial and time consuming process as in gold stud bonding. By electroplating copper columns through a resist mold and then also capping the columns with gold to facilitate the thermo-sonic process, higher throughput and cost effectiveness can be realized. Electroplated copper columns are covered by an electroplated diffusion barrier of nickel and then the thermo-sonic bonding gold cap. One advantage of this process is that no chip side processing is necessary prior to bonding itself. Once the columns are gold capped, they are flip-chip aligned to the aluminum pads on the chip and then bonded under force, ultra-sonic action, and elevated temperature (as shown in Figure 2.10). The stage temperature was chosen to be fixed at 200°C for all of the work reported. For optimization of the thermo-sonic process,

ultrasonic power, bonding force, and time were used as variables and maximum shear stress of the bonded pillars as the desired output.

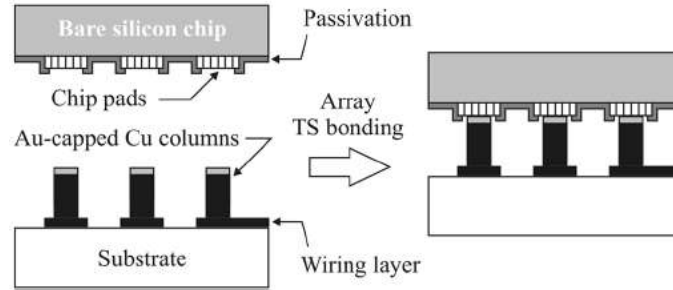


Figure 2.10: Thermo-sonic bonding process for Cu columns

By using a Box-Behnken design of experiments approach, a surface response for the three variable system was performed and the bonding process optimized. The optimized process used ultra-sonic power between 8 and 16 W and time of 100 to 300 ms. The pressure applied was 0.012 to 0.013 g per μm^2 bonded. Finally the arrays were bonded to quartz test substrates and put under a few basic thermo-mechanical stability tests. While these tests served as an initial evaluation of the system under stressed conditions and without underfill, it did not reflect the more important case for flip-chip packaging with FR-4 type substrates since the CTE of quartz is much closer to that of silicon. Therefore, further testing of the system with higher CTE boards must be done in the future to accurately assess the thermo-sonic column system as a feasible solder-free solution for flip-chip packaging.

2.3.3 Compliant Gold Bump Interconnects

Copper wafer bonding and Surface Activated Bonding discussed above are solid-state bonding techniques to create connections between copper surfaces. Watanabe et al. have developed a novel process utilizing thermo-compression similar to the copper wafer bonding process that uses gold as the interconnect material.[38.39] By taking advantage of the mechanically soft character of gold and also its exceptional capability to electroplate unusual geometry, the compliant gold bump interconnect was developed. By using an undercut photoresist pattern as the electroplating mold cone shaped gold bumps can be created. Due to the extremely small cross-section of the tip of the cone, the material can be made to yield and flatten during the thermo-compressive bonding cycle. Figure 2.11 shows an image of the cone shaped Au bumps and the process steps for bonding the cone shaped gold bumps to the plated gold pads. The advantage that the cone bump has versus simply bonding flat surfaces is that is it not necessary for the surfaces of chip and substrate to be perfectly parallel. Each individual bump can flatten as much as needed to compensate for the non-planarity between chip and substrate. Additionally, the sharp tipped gold cone also allows for underfill material to be dispensed directly onto the substrate prior to bonding. The sharp tip of the cone will then penetrate the underfill film and make metallic contact with the pad perfectly excluding the dielectric material. As the cone plastically deforms under pressure, the underfill continues to be forced out of the interconnect geometry. This allows for simple fabrication technique with high potential for thermo-mechanical reliability of the bonded joint.

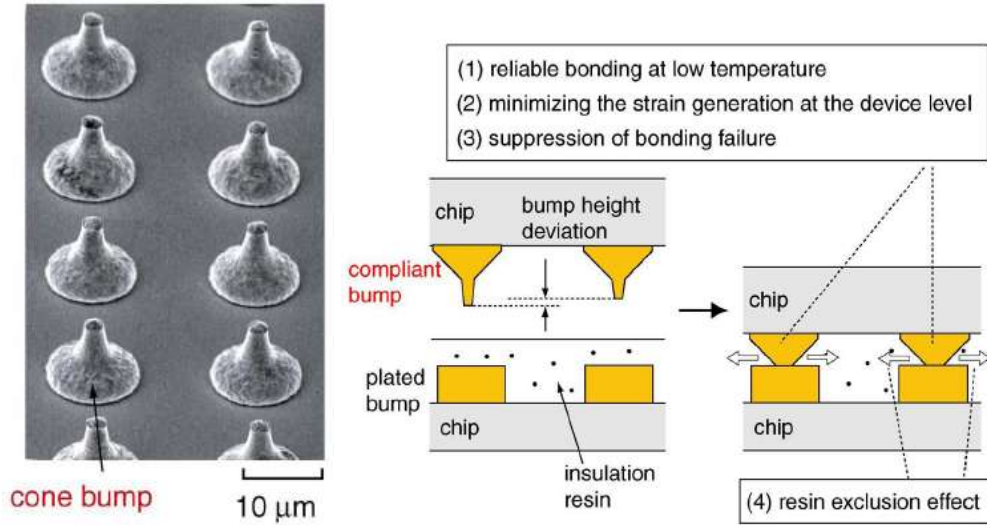


Figure 2.11: (left) SEM image of cone shaped Au bumps and (right) process steps for bonding the Au bumps to Au pads utilizing compliant bump tip

Watanabe et al. utilized both pressure and temperature to generate a solid bond between the Au compliant structures and the underlying pads.[38.39] The reported values were for chip side heating up to 300°C and substrate side heating to 100°C. Force applied to flatten the compliant bumps was reported to be 0.5 kgf per bump bonded. The structures showed confirmed electrical connection by daisy chain testing. The reported test structure consisted of 10 μm base diameter cone bumps with pitch of 20 μm. For a 2mm x 2mm test vehicle these dimensions lead to 10,000 I/O on a single test chip. This I/O density is remarkable compared to current solder interconnect methods. However, the use of gold as the interconnect material is not the most desirable alternative material. Since gold is significantly more expensive than copper or solder, it will be less likely to be used for manufacture due to cost of materials alone. In addition electroplating of gold is much more demanding for waste disposal versus typical electroplating used for copper.

2.3.4 Electroless NiB Interconnects

Electroless copper plating for the creation of chip-to-substrate area array interconnects has been mentioned previously. Recently, a new approach to creating peripheral array interconnects utilizing an electroless plating technique has been reported by Yokoshima et al.[40] In this technique NiB is electrolessly deposited between copper pads to generate an electrical connection. One of the most exciting aspects of this work is that the plating is done without need for any patterned material or seed layer to direct the plating process. Taking advantage of previously reported studies on “extraneous” deposition causing bridging between metal pads during electroless plating, this technique instead utilizes “extraneous” deposition to directly grow a conductive link between chip and substrate pads. Many researchers have analyzed problems dealing with plating creating bridged links between adjacent structures on surfaces.[41,42] While most of the previous work was done to minimize or eliminate the effects of plating that generated these bridged connections, this technique attempts to harness this ability and use it to create desired connections.

Yamaji et al. have shown that by carefully choosing the correct pitch between interconnects and also the vertical spacing between the pads to be bonded, successful connections can be achieved.[43] For the demonstrated 5 μm wide copper pad test system, pitches less than 20 μm led to plating between neighboring pads and therefore undesirable electrical connections. However, when the pitch was 20 μm or greater plating did not take place between adjacent pads on the surface. Also, it was found that the pad-to-pad distance to successfully join vertically aligned pads was 5 μm or less. At these vertical separations NiB successfully deposited on the insulating material and creating a measurable electrical connection between the pads (as shown in Figure 2.12).

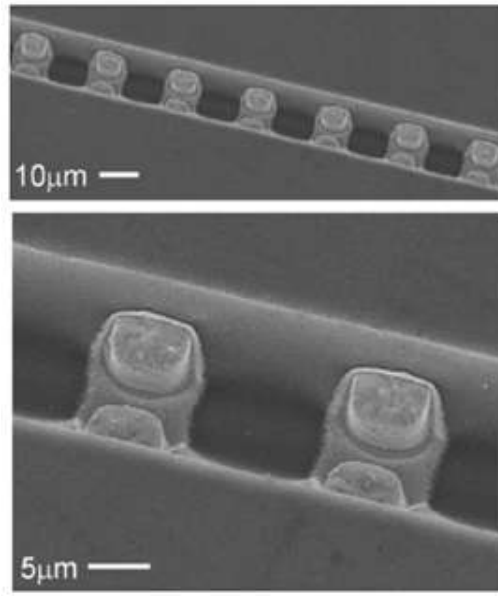


Figure 2.12: Electroless NiB bonding between Cu pads

While the exact mechanisms of the “extraneous” electroless deposition onto the insulating material are not known, it appears to be effective in joining pads to make electrical connections. One critical drawback of this process is it does not appear to be able to create area array connections due to the geometry for the proposed fabrication scheme. Still creating such fine pitch peripheral array connections effectively and efficiently without the need for solder is important. Future research may elucidate a path for this technique to be applied to area array type connections.

2.4 Distant Future Needs for Chip-to-Substrate Connections

2.4.1 Ultra-high Off-Chip Frequency and High Bandwidth Operation

The ITRS projects that in the future off-chip operating frequency will increase dramatically. By the year 2020, the projections are for operating frequency to reach 72.4 GHz. To operate at such high frequency, the methods of interconnecting the chip to substrate must be carefully considered. Basic pin-type connections used today will not perform as well and may need to be replaced with more electrically high performance connections. There have been many methods proposed to increase performance of the chip-to-substrate connection for high frequency.

2.4.1.1 Coaxial Interconnects

Wu et al. have proposed a coaxial chip-to-substrate connection that showed promising high frequency operation up to 80 GHz based on simulations.[44] Utilizing build-up processing, a ‘C’ shaped ground connector was formed in conjunction with a center signal conductor on both the chip and substrate surfaces. Then, the two pieces were aligned and bonded to form the coaxial type connection. Figure 2.13 schematically shows the vertical coaxial interconnect fabrication and assembly processes. Experimental measurement of the high frequency performance was made by attaching the test structure to coplanar waveguides on the substrate and chip surfaces. Wu et al. have experimentally fabricated and tested the proposed vertical coaxial structures.[45] Testing the return and insertion loss S-parameters from 0 to 70 GHz was performed. Based on the results, the simulations characterized the interconnect scheme effectively. The loss caused by adding underfill to the system was greater as expected. However, the coaxial connections still showed low return and insertion loss of 13.7 dB and 0.9 dB respectively at 60 GHz. Coaxial type connections such as these could be promising for operations at such high frequencies as projected for the future by the ITRS.[5]

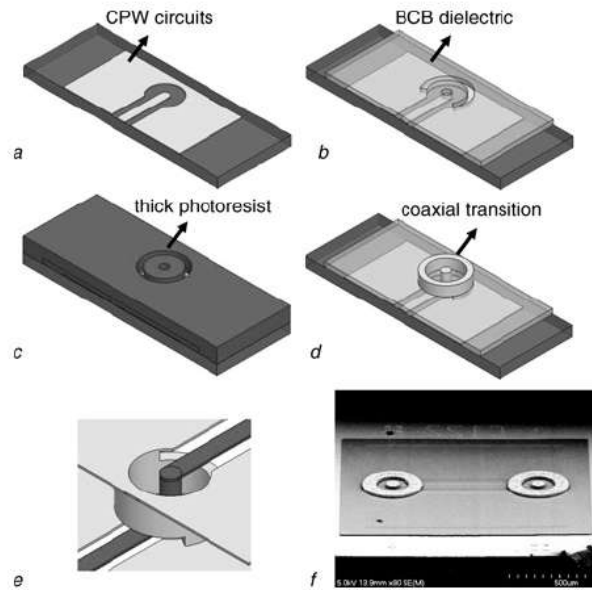


Figure 2.13: Vertical coaxial interconnect fabrication and assembly

2.4.1.2 Electrical and Optical Interconnects

The ITRS projects that by the 18-nm generation node high-performance chips will dissipate 200 W, require 200 A of supply current, and have clock frequencies greater than 70 GHz. These high power dissipation requirements mean that minimizing the power distribution network IR drop and noise are critical. In addition, the signaling network will be limited by increased losses from impedance mismatch, cross-talk, and organic substrates. One solution to such challenges is the incorporation of optical communications between the chip and substrate.[46,47]

By combining the high bandwidth optical I/O with typical electrical I/O connections, Bakir et al. have demonstrated a current CMOS fabrication compatible hybrid interconnect structure.[48] One of the proposed structures comprises optical connections made by polymer pins serving as vertical optical connections, with traditional solder balls providing electrical connections. By using the polymer pins for optical connections, versus the typical free-space optical I/O, the system is fully

compatible with underfill dispensing for thermo-mechanical reliability. Bakir et al. also proposed a more integrated structure that is termed “dual-mode” pin connections.[48] For this structure the polymer pins are metallized on the exterior surfaces (as shown in Figure 2.14). By having an electrically conductive path incorporated onto the polymer pillars, both electrical and optical connections can be made by each structure. This could potentially lead to high I/O density, but having the metal film coating the exterior of the polymer structure will limit its mechanical compliance. Therefore, there is a trade-off to be made between the electrical performance and mechanical compliance. Bakir et al. showed that compliance increases with reduced metal thickness, and that electrical resistance increases with metal thickness.[48] For practical use the dual-mode pin would have to be carefully designed based on the application specific electrical and mechanical performance needs.

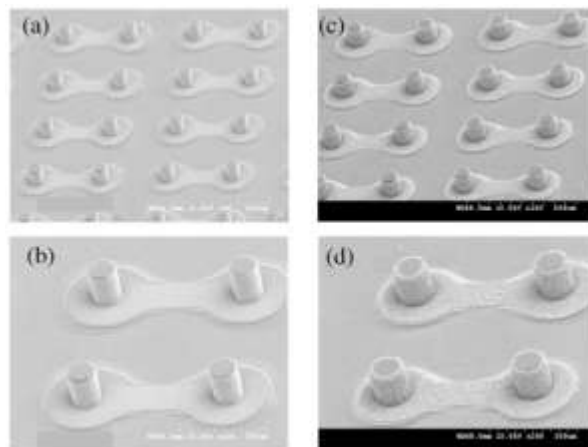


Figure 2.14: SEM images of dual-mode metal clad polymer pins with (a and b) Au clad and (c and d) solder plated onto structures

CHAPTER 3

EXPERIMENTAL METHODS AND TECHNIQUES

3.1 Fabrication of All-Copper Test Structures

The fabrication process flow diagram is shown in Figure 3.1. A seed layer consisting of Cr/Cu/Ti (50nm/500nm/10nm) was DC sputtered onto a bare <100> 4" Si wafer. Then, a Unaxis PECVD system was used to deposit 1.5 μm of silicon dioxide at 250°C on top of the Ti layer. Microposit SC1813 photoresist (Shipley Corporation) was spun on the silicon dioxide surface. After photo-patterning the photoresist layer, buffered oxide etch (BOE) was used to etch the SiO_2 and Ti layers in the exposed areas down to the underlying Cu seed layer. Remaining photoresist was removed by acetone rinsing. Next, a thick layer of Avatrel 2195P polymer (Promerus LLC, Brecksville, OH) was spun onto the sample surface. The spin speed for the polymer was 500 RPM for 60 seconds. After spin-coating, a 100°C soft-bake was performed on a hotplate for 40 minutes. The Avatrel layer was then photo-patterned using 250 mJ/cm^2 dose at 365nm wavelength. Following exposure a post-exposure bake was applied in an oven at 100°C for 20 minutes. Then, the layer was developed in BioAct EC-7R Defluxer for 30 seconds immersed in an ultra-sonic bath. The polymer pattern generated high aspect ratio hollow core molds for copper pillar electroplating.

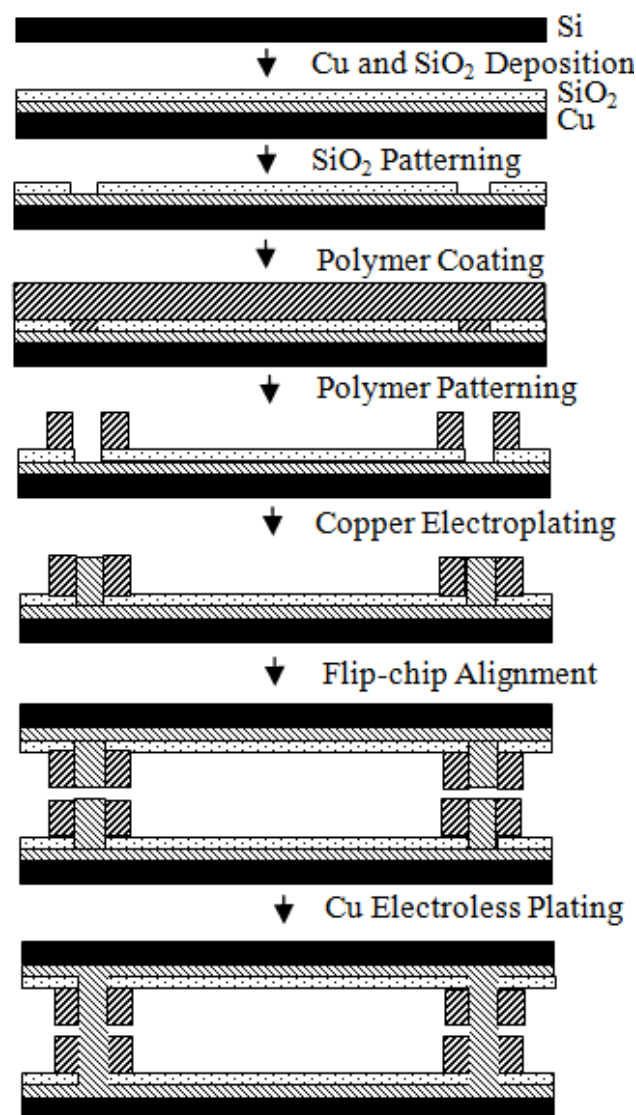


Figure 3.1: Fabrication flow for fabrication of all-copper interconnects structures

After the patterning steps copper pillars are electroplated to fill the polymer molds. The electroplating solution contained 30 g/L CuSO₄, 52 g/L H₂SO₄, 40ppm Cl⁻, 0.5vol% brightener agent, and 0.5vol% carrier agent. Electroplating was carried out in a homemade cell at 2 mA/cm² for 20 hours, using a phosphorus doped copper anode. Electrical current was supplied via a Pine Instruments AFR-DE5 Potentiostat. After electroplating, test chips were then diced and flip-chip aligned in a RD Automation M-

10A flip-chip bonder or alternatively in a FineTech Fineplacer bonder. Aligned samples were then temporarily held together with a low temperature melting wax.

The aligned samples were then placed into a copper electroless plating bath. The bath used was Circuposit 3350 from Shipley Corporation. In this bath the reducing agent is formaldehyde (2 g/L), complexing agent is EDTA (ethylenediaminetetraacetic acid) (35 g/L), and also contains sodium hydroxide reaching a pH of 12.5. The electroless plating process proceeded at room temperature for 18 hours with stirring and nitrogen purging. After electroless plating the samples were annealed in a nitrogen environment for one hour at various temperatures. In addition some samples were annealed after electroplating but prior to the flip-chip alignment, electroless plating, and post-bonding anneal steps.

To evaluate the effect of height mismatch, polystyrene micro-spheres (Polysciences Megabeads) with a diameter of $125\ \mu\text{m} \pm 2.3\ \mu\text{m}$ were dispersed from a DI water solution with 1 wt% solids onto the sample surface. These micro-spheres served to set a known stand-off distance between the sample surfaces illustrated in Figure 3.2. To create different separation distances between the pillar top surfaces, different height pillars were electroplated onto the samples of 30, 40, and 50 μm , leading to separation distances between the pillar surfaces of approximately 65, 45, and 25 μm respectively.

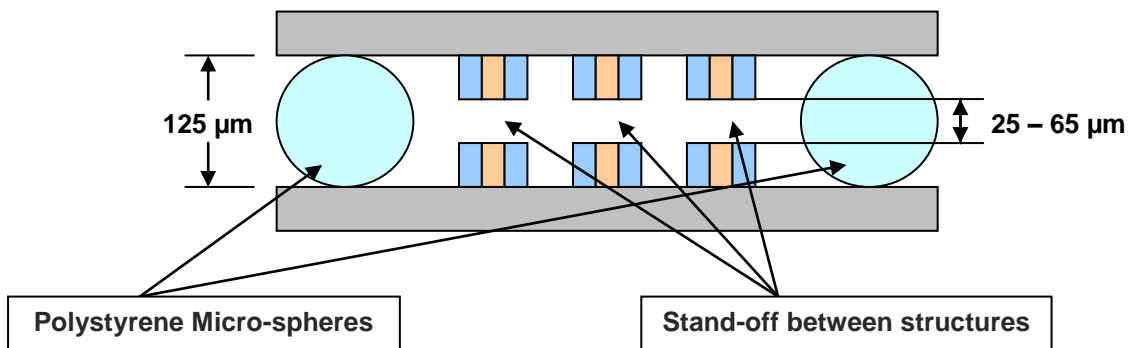


Figure 3.2: Illustration of setting stand-off distance with polystyrene micro-spheres

After annealing samples were shear force tested by fixing the base of one chip and applying a shear load to the other using an Instron 5842. These results were then converted to shear stress by using a total surface area average of interconnects placed under load.

To fabricate test samples on the printed circuit board materials an alternate approach was taken show in Figure 3.3. FR-406 (FR-4) from Isola Global was received with copper laminated to the surface. On top of the copper layer a thin Ti adhesion layer, 10 nm, was sputtered onto the surface. Then, a thick layer of Avatrel 2195P was spin-coated to 50 μm thickness. This layer was photo-defined to create openings for pillars. Buffered oxide etch was used to remove the Ti from the holes. Then, the previously described electroplating process was used to build up the copper pillars. Finally, the substrates were cut into 10mm x 10mm test samples for bonding to fabricated silicon test chips.

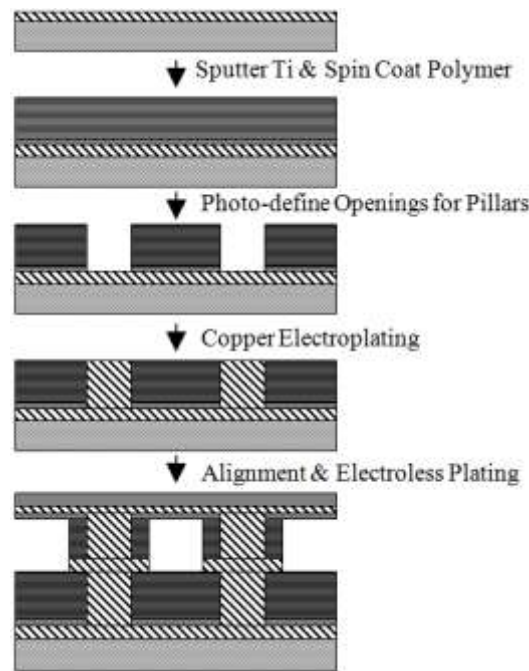


Figure 3.3: Substrate side fabrication flow diagram

3.2 Polymer Collar Fabrication

The effects of increased modulus of the polymer collar were experimentally verified. Copper pillars were fabricated with three different photodefinable polymer collars, each with a different elastic modulus. The samples were bonded via the electroless copper plating and annealing process, as described previously, and then shear tested to investigate the mechanical strength.

The fabrication process for all-copper was previously described. Fabrication parameters for the three materials: Avatrel 2195P (Promerus LLC, Brecksville, OH), Avatrel 8000P (Promerus LLC, Brecksville, OH), and SU-8 2025 (MicroChem Corp., Newton, MA) are summarized in Table 3.1. Each polymer was used to create high aspect ratio polymer collar plating molds with different mechanical properties. SEM images of copper pillars fabricated with each of the three systems are shown in Figure 3.4. Based on reported values for the elastic properties of these three materials, a range of modulus values between 0.5 and 4.0 GPa was expected. All of the samples tested were annealed at 180°C for 1 hour in a nitrogen environment.

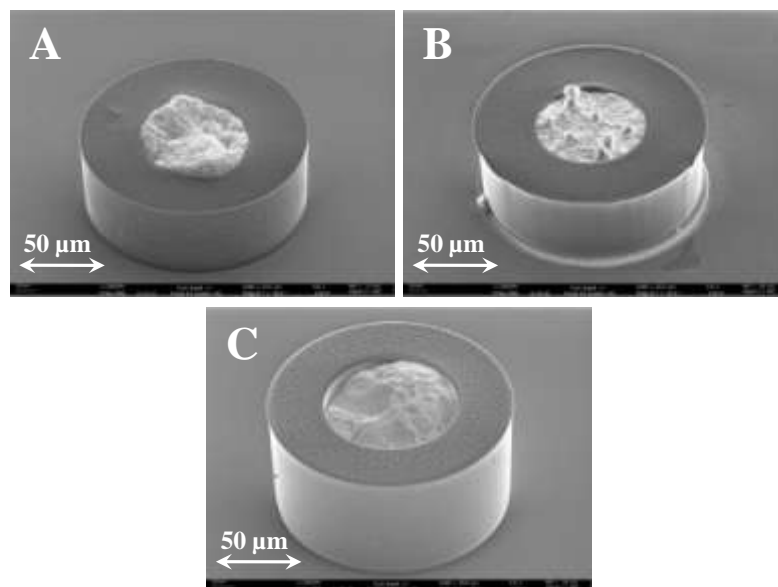


Figure 3.4: SEM images of the three different collar systems after copper electroplating

(A = Avatrel 2195P, B = SU-8, C = Avatrel 8000P)

Table 3.1: Polymer collar processing conditions for the three photodefinable systems

Polymer Collar Systems Processing Conditions Summary / Comparison					
Material	Soft Bake	Exposure (365nm)	Post-Exposure Bake	Development	Reported Elastic Modulus (GPa)
Avatrel 2195P	30 min, 100°C	200 mJ/cm ²	20 min, 100°C	Ultrasonic, BioAct Defluxer	0.5
Avatrel 8000P	5 min, 100°C	450 mJ/cm ²	5 min, 100°C	Puddle, Aqueous Base (Shipley MF-319)	2.5
SU-8	2 min, 65°C 5 min, 95°C	320 mJ/cm ²	Start 32°C, Ramp 10°C/min to 95°C, Hold 3 min, Cool to 42°C takes 20 min	Puddle, PGMEA Solvent	1.5 - 4.5

3.3 Nanoindentation for Polymer Mechanical Property Characterization

Mechanical characterization of the three polymer collar materials was performed using a Hysitron Triboindenter to obtain the reduced elastic modulus and hardness of each polymer as-processed with the all-copper process steps. Since the processing time and temperature was not the optimum cure recommended for each photodefinable system, the modulus of each material may vary from reported values which utilize the recommended baking and curing conditions. The indentation experiments were performed with a Berkovich diamond tip using the method reported by Kranenburg et al. for polymer materials characterization.[49] Each material was indented ten times from 300 μN to 3000 μN maximum load. The first three indentations (300, 600, 900 μN maximum loads) were omitted from calculating the results to further reduce the influence of drift and also due to the maximum depth at these loads being close to the minimum calibrated depth for the contact area function. Fitting for the unload data was performed via the method of Oliver and Pharr using a power law relationship.[50] From the fitted data and the contact area function, the reduced elastic modulus of each material was calculated. The relationship between reduced modulus and the nanoindentation data is given by Equation 3.1. The hardness of each material was calculated using Equation 3.2. Nanoindentation data for the three polymer systems at the highest tested load (3000 μN) are shown in Figure 3.5.

$$E_r = \frac{\sqrt{\pi}}{2} \frac{S}{\sqrt{A(h_c)}} \quad (3.1)$$

Where E_r is the reduced elastic modulus, S is the contact stiffness, and $A(h_c)$ is the contact area as a function of the contact depth h_c .

$$H = \frac{P_{\max}}{A(h_c)} \quad (3.2)$$

Where H is the hardness, and P_{\max} is the maximum load.

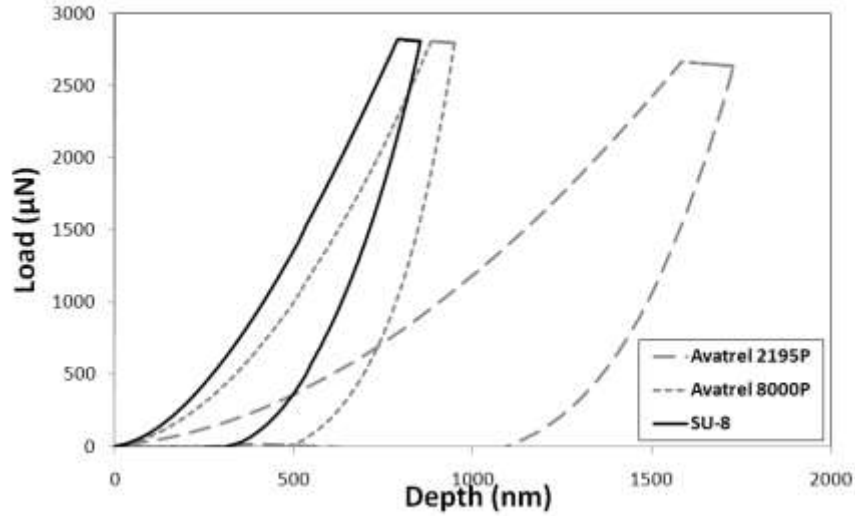


Figure 3.5: Load response for the three polymer collar materials tested at a maximum load of 3000 μN

3.4 Electroless Gold Deposition and Bonding

To compare the copper process to an alternative metal, electroless gold deposition was used. Here, a standard electroless gold bath described by Okinaka et al. [51] was used to deposit gold between the copper pillars. Gold deposition proceeded at 70 C for approximately 18 hours. However, the initial copper surface is a poor catalyst to start the electroless gold process. Therefore, a homemade electroless palladium bath was used to activate the samples and allow gold deposition to proceed. The electroless palladium solution was based on a previous in-house electroless platinum solution [52] and was operated at 70 C. Palladium was allowed to deposit until a coating was visible on the

copper pillar surfaces (typically ~30 seconds or less). The compositions for the gold and palladium baths are given in Table 3.2. After electroless gold plating was completed, annealing was performed at 180 C for 1 hour in nitrogen ambient to compare to the all-copper process. The resulting bonded samples were then cross-sectioned and analyzed via SEM and EDS.

Table 3.2: Bath compositions for electroless gold and palladium deposition

Electroless Au		Electroless Pd	
Component	Concentration (g/L)	Component	Concentration (g/L)
KAu(CN) ₂	6.00	PdCl ₂	1.25
NaCN	10.00	HCl	33.00
NaOH	8.00	5, sulfosalicylic acid hydrate	1.00
NaBH ₄	15.00	Sodium benzene 1,3 disulfonate	0.50
		Sodium 1,3,6 naphthalene trisulfate tribasic hydrate	0.25
		Hydrazine dihydrochloride	3.75

3.5 Copper Line Capacitor Fabrication and Testing

Copper lines were fabricated on glass substrates to electrically study the deposition process. Utilizing standard microfabrication techniques copper lines were fabricated in a comb capacitor type structure as shown in Figure 3.6. Once the samples were fabricated, insulated copper wiring was attached to the probe pads for electrical contact. While the electroless deposition process took place, the resistance of the opening between the two copper lines was measured via the four-point probe technique. The four-point probe and a high resolution voltmeter/ammeter were used to minimally interfere with the plating process. The probe was shut down between measurements to avoid disturbing the electroless deposition mixed potential.

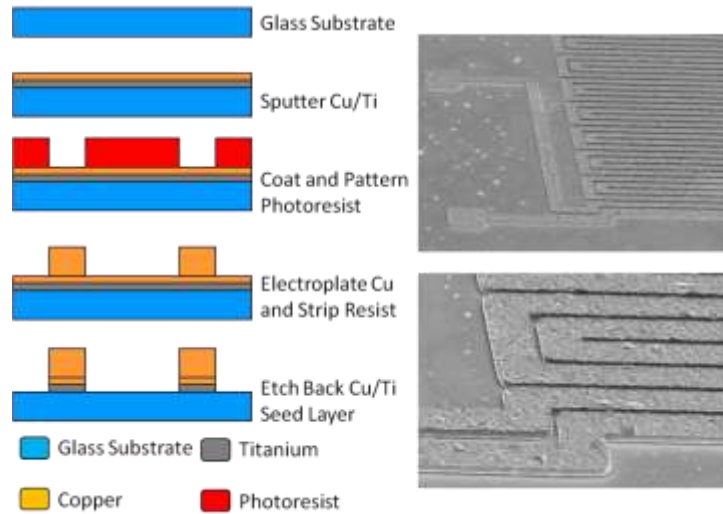


Figure 3.6: (left) Fabrication flow for copper line capacitors and (right) sample SEM image of fabricated structures

3.6 Electroless Copper Deposition with PEG Suppression

All of the specimens used for this study utilized the improved photodefinable polymer collar material Avatrel 8000P.[53] After fabrication and temporary flip-chip attachment, the aligned samples were then placed into a copper electroless plating bath. The bath used was again based on Circuposit 3350 from Shipley Corporation. In order to investigate the inhibiting effect of PEG on our samples, electroless plating proceeded at 70 C. Initial deposits were performed on blank copper surfaces and the deposition rate was characterized as a function of PEG concentration in the bath. Based on these results the copper pillar flip-chip samples were plated for 3, 6 and 12 hours at concentrations of 1, 2 and 3 ppm respectively of PEG with stirring and air purging. The PEG was used as received from TCI with a molecular weight of 4000 grams per mol.

CHAPTER 4

FABRICATION AND CHARACTERIZATION OF THE ALL-COPPER PROCESS

4.1 Overview

In this chapter a novel fabrication process has been developed and characterized to create all-copper connections from chip-to-substrate. Copper electroless plating followed by low temperature annealing in a nitrogen environment was used to create an all-copper bond between two copper pillar surfaces. No solder materials were required to create the bond between pillars. Using this technique, bond strength exceeding 165 MPa was realized using processing temperatures of 180° C. The ability to fuse two copper surfaces at modest temperatures (below 200°C) and pressure is demonstrated. During the anneal process a significant microstructure transformation in the bonded copper-copper interface was observed and correlated with an increase in the bond strength at anneal temperatures of 180°C and greater. The process was characterized with respect to xy in-plane misalignment of bond sites and successfully overcame misalignment greater than the dimensions of the parts bonded. Capabilities in handling height mismatch between bonding surfaces was also assessed and shown to bond mismatches of 65 μm or less. Height mismatch was shown to be important in creating optimal quality geometry in the copper-copper bond. Successful bonding between silicon test chips and organic printed circuit board materials was also performed showing no observable degradation of the organic board material. This work was previously published in the Journal of the Electrochemical Society.[54]

4.2 Results

4.2.1 Bonding and Shear Testing

The critical technological and scientific advance of this work is the copper-to-copper joint generated by the low annealing temperature. Minimizing the temperature excursion necessary to create adequate bond strength is desirable to allow for processing with minimal effect on the integrity of the organic substrate materials and other temperature sensitive components. In order to assess the effects of the anneal temperature on bond strength; samples were annealed for a range of temperatures from 180°C to 400°C. The purpose for choosing temperatures as high as 400°C was to decompose the Avatrel polymer molds for direct observation of the all-copper bonded system. The results of these tests are summarized in Table 4.1. It can be seen that the surface averaged shear stress required to fail samples between 200°C and 250°C all follow a general trend of increased allowable stress with increased anneal temperature. However, the results at 400°C deviate from this trend due to the decomposition of the polymer mold supports at this temperature, thereby reducing the ability of the system to dissipate stress.

Table 4.1: Effects of anneal temperature on the shear strength of the bond

Anneal Temperature (°C)	Maximum Shear Stress** (MPa)
400*	148
250	189
220	132
200	119
180***	165
150	< 20
25	< 20

All annealing performed for 1 hour

** Avatrel is completely decomposed*

*** Based on pillar area and number of pillars*

**** Annealed prior to bonding at 250C, 1hr*

For all tests conducted between 200°C and 400°C the point of failure was at the pillar-to-surface interface and not in the electrolessly plated pillar-to-pillar bond. This shows that the trend in reduced allowable stress is actually measuring the improvements in adhesion of the pillar to the surface due to increased anneal temperature. To quantify the limits of the strength of the electroless plated bond, an additional anneal step was added prior to flip-chip alignment and electroless plating at 250°C for 1 hour. The pre-bonding anneal step enhanced the pillar-to-surface adhesion while having no direct impact on the pillar-to-pillar bond. After electroless plating the sample was annealed at 180°C. Upon shear testing it was observed that the point of failure was the pillar-to-pillar electroless plated interface. This implies that the allowable shear stress the electroless plated bond could withstand was approximately 165 MPa. A bond yield strength of 165 MPa is consistent with the previous results using a single 250°C anneal step after the bonding process. The pillar-to-surface adhesion measured was greater at approximately 189 MPa. Withstanding shear stress up to 165 MPa is significant when compared to the yield stress of bulk electrodeposited copper of 225 MPa [55], being about 75% of this value. Further samples were annealed at 150°C for 1 hour but were not quantitatively measured since the samples failed during mounting for shear force testing. Unannealed samples failed during mounting and were also not quantified.

In addition to testing the mechanical properties of the annealed interconnects, it is also important to characterize the microstructure effects of the anneal process on the pillar-to-pillar bonded interface. To understand the morphological changes taking place during annealing, cross-sections were made of structures both prior to and after the annealing process was performed. Figure 4.1 is a cross-section of the two joined pillars after the plating process but before annealing. In Figure 4.1 the two pillars are labeled as Cu and each silicon test surface is also labeled as Si. There is a distinct interface between the two electroless plated regions. The interface between the pillars is evident as a dark crevice between the two copper regions. The fragility of this poorly mixed interface was

observed when attempts were made to quantify the shear stress required to break the unannealed interconnects. Handling of the parts to mount for shear testing was sufficient to break any bonding present.

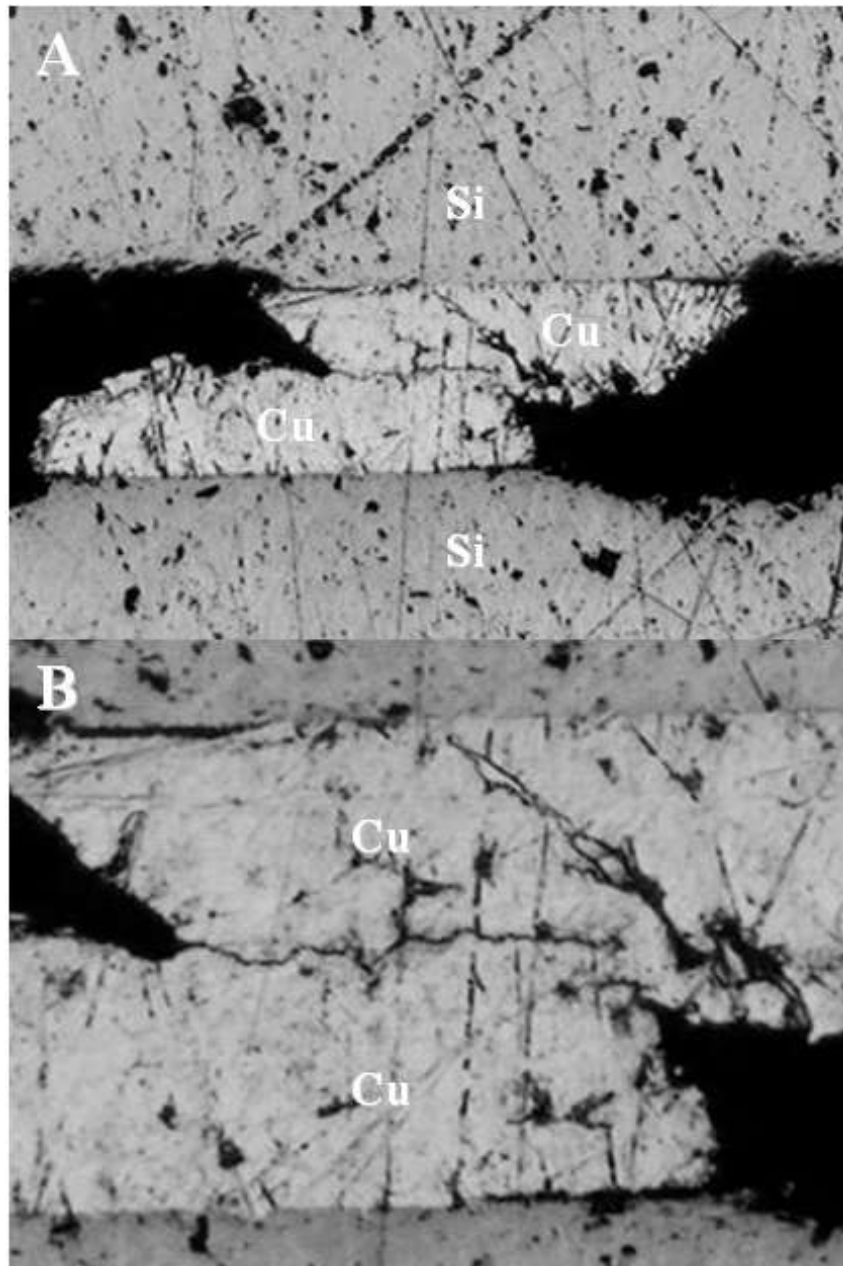


Figure 4.1: Cross-section image of bonded copper pillars prior to annealing (a) full view
(b) higher magnification of bonding interface

Cross-sections were made after annealing for a shortened period of time at lower temperature (150 ° C) to analyze the change from the distinct unannealed interface to the continuous smooth copper observed in the fully annealed structures. In Figure 4.2a, the interface is still present after 30 minutes at 150°C. After an additional 30 minutes at 180°C (Figure 4.2b) the interface has been removed entirely and the copper bonding process has completed. For another sample annealing was done at 150°C for 2 hours. Cross-sections of this sample are shown in Figure 4.3. The interface remained at all bond sites observed for this process condition. This shows that even using a significantly longer anneal time, the interface is not removed at 150°C. However, all samples tested with anneal temperatures of 180°C or greater showed the interface removed. These experiments demonstrate a minimum temperature requirement for bonding between the two plated regions in the range of 180°C. Without sufficient thermal activation the two copper surfaces will not merge even at the longer anneal time of 2 hours.

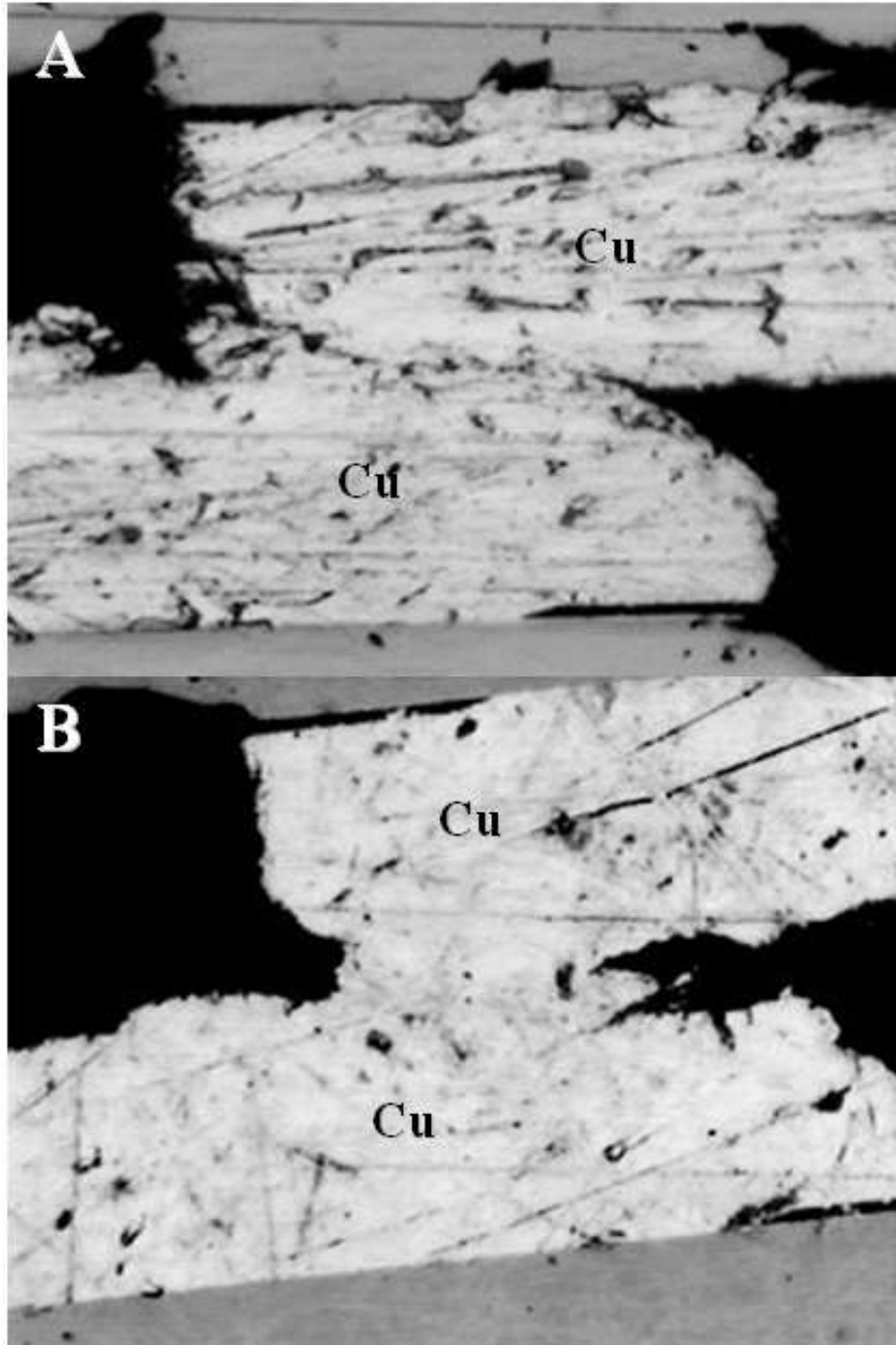


Figure 4.2: Cross-section after annealing at (a) 150°C for 30 min. and (b) 180°C for an additional 30 min.

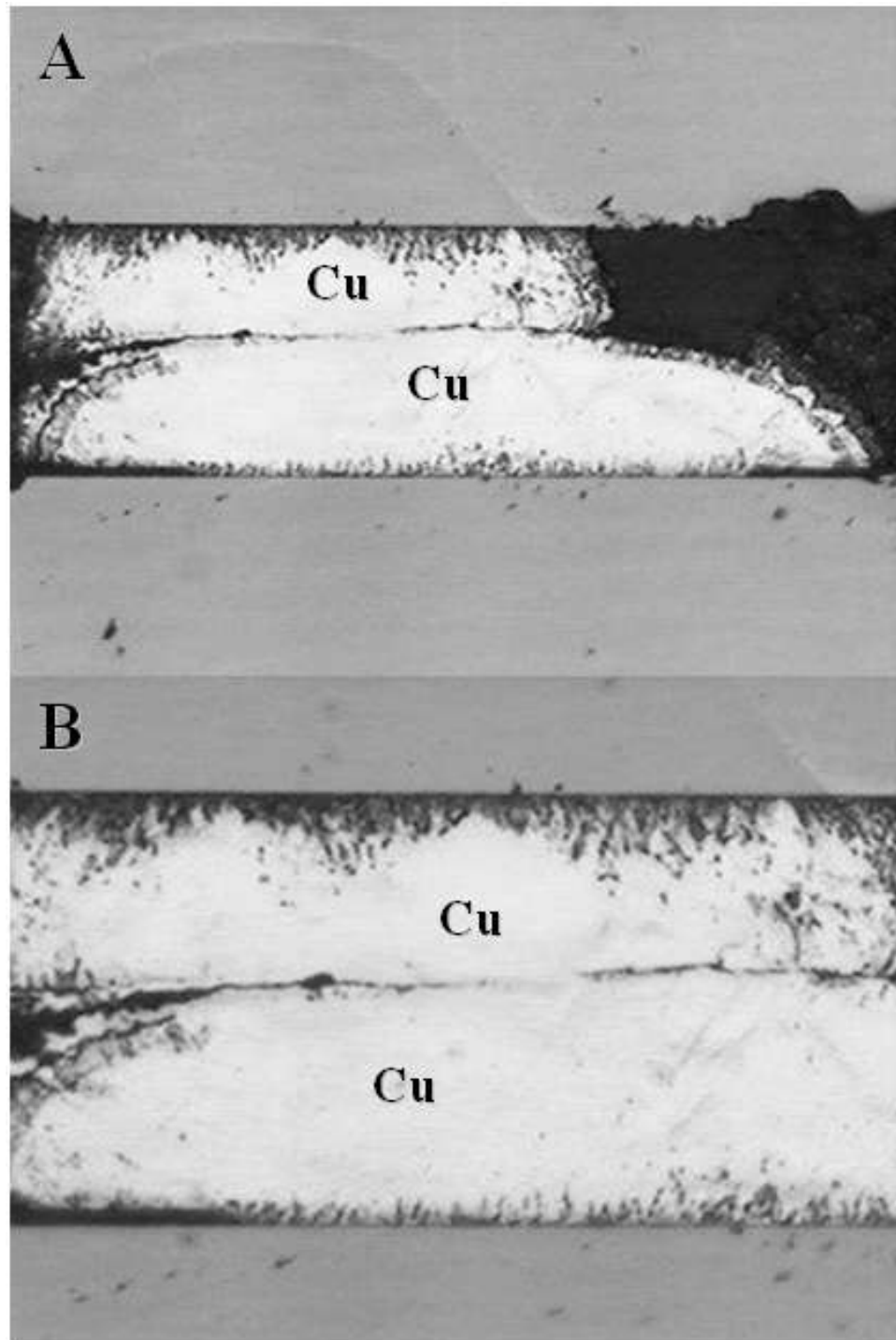


Figure 4.3: Cross-section after annealing at 150°C for 2 hours

4.2.2 Misalignment Dexterity Assessment

In addition to optimizing and characterizing the annealing process, assessment of process capabilities to tolerate planar xy-misalignment was also performed. Solder exhibits excellent ability to account for misalignment between contacts during the reflow process. This property allows for higher throughput and yield for the assembly process. Any novel chip-to-substrate interconnect system must have properties to account for planar misalignment comparable to solder in order to be cost effective and viable. To test the planar tolerance, copper pillars were intentionally misaligned and then taken through the electroless plating and annealing process. Figure 4.4 shows two pillars that were successfully bonded despite misalignment greater than the diameter of the pillars themselves, which exceeds the capabilities of solder. The bonded set survived destructive shear testing, showing that the pillar-to-pillar bond was still stronger than the pill-to-surface adhesion despite its significantly reduced cross-sectional area, and non-uniform geometry.

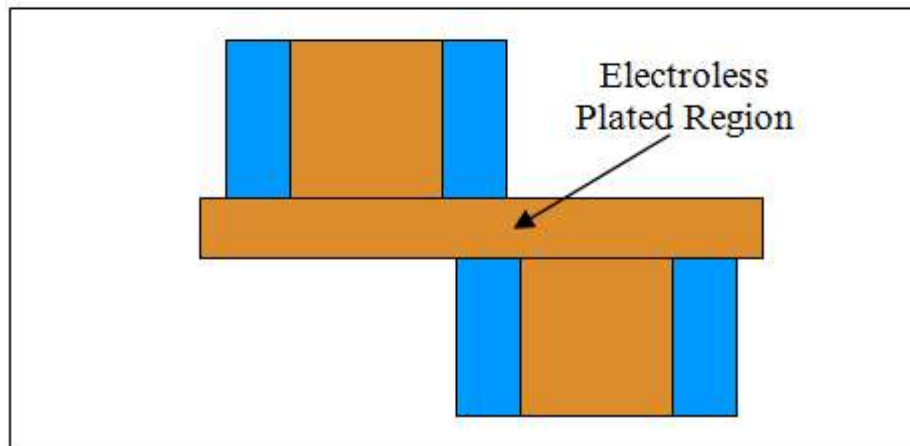
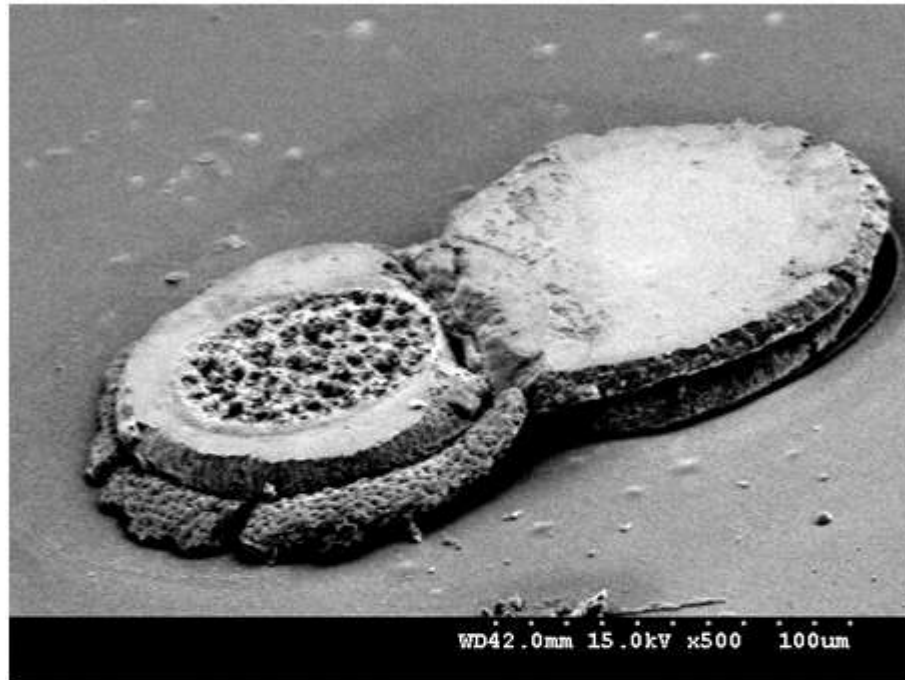


Figure 4.4: (above) SEM image and (below) concept of planar misalignment greater than pillar diameter

The solder reflow process has unique capabilities to overcome the non-planarity of organic substrates and either elongate or flatten as necessary to bond the chip to the package. Assessing the z-axis height mismatch the all-copper process can overcome is important in characterizing its dexterity versus traditional solder processing. Figure 4.5 shows SEM images of the results of testing separation distances of approximately 25, 45,

and 65 μm . The time each type of sample was in the electroless plating bath was held constant at 24 hours. Looking at Figure 4.5 it can be seen that the smallest separation distance led to significant outward plating beyond the diameter of the pillars bonded. For the intermediate separation distance, the joint appears very uniform and minimal plating beyond the diameter of the pillars is observed. Finally, at the largest separation distance the plated joint is entirely contained within the diameter of the structures bonded. That the largest separation led to an interior plated joint was surprising. It was expected that the plating rate would be less in the center due to the transport difficulties in the system and consumption of reactants. However, this type of plated joint was observed over large areas of multiple samples. The plating rate was fastest in the center and was the location for bonding. An example of an array of bonded structures showing this is found in Figure 4.6. From the results of this test it is evident that having z-axis separation in the proper range can lead to improved final geometry of the bonded structure which will be desirable as off-chip frequency increases to minimize reflections and signal loss. All three stand-off distances survived destructive shear testing.

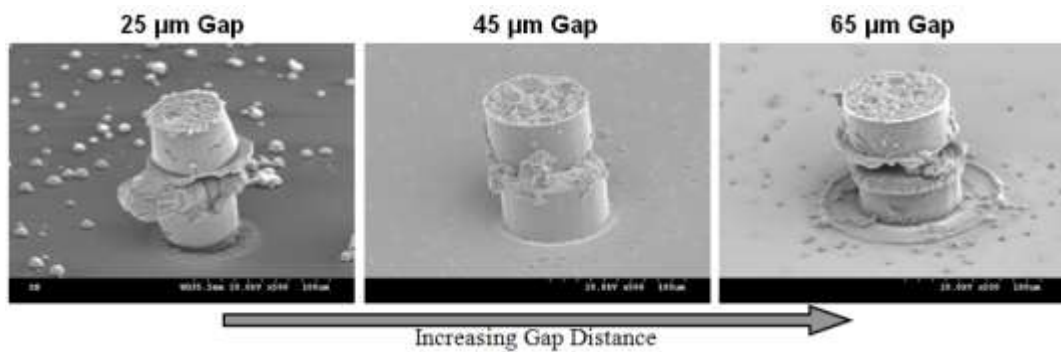


Figure 4.5: SEM images showing the effects of increasing separation distance between pillar surfaces at distances of: (left) 25 μm (middle) 45 μm (right) 65 μm

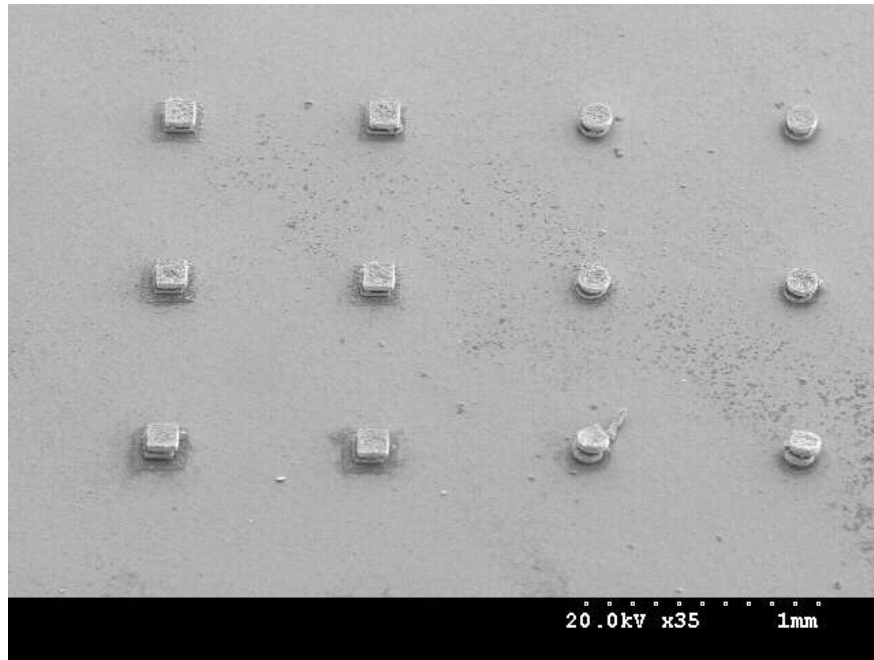


Figure 4.6: SEM image showing bonded and shear tested structures at the largest separation distance

4.2.3 Bonding between Si and Organic Substrate

This process is intended to bond silicon chips to organic substrate packages. Therefore, samples were prepared with copper pillars on FR-4 organic substrates and additional silicon test chips. Samples were made using the flip-chip alignment, electroless plating, and low temperature annealing process described above. An anneal temperature of 180°C for one hour was used. Bonding between silicon and the organic materials is unique versus the silicon-to-silicon bonding tests in that the materials no longer have the same coefficient of thermal expansion (CTE). The CTE of Si is 3 ppm/°C versus 14 ppm/°C for FR-4 and 15 ppm/°C for BT. During the annealing process, the copper interconnects will be under shear stress conditions. Brongersma et al have shown that copper films under stress during recrystallization can exhibit unusually large grain growth termed super secondary grain growth.[56] Shear loading conditions could potentially be helpful to the bonding process and encourage grain growth in the bonded

region. After annealing, the samples were shear tested and compared to silicon-to-silicon bonded samples annealed at the same temperature.

The silicon-to-board bonded samples exhibit different failure characteristics versus silicon-to-silicon bonding. Since the Avatrel is no longer a single polymer collar surrounding the copper pillar on the organic substrate, but instead a continuous polymer film, it can no longer detach from the surface easily during shear force testing. Therefore, the stress failure takes place in two steps. First, the copper pillar is broken from the copper laminate surface (pillar-to-surface adhesion). Then, the pillar is pulled out from the polymer film and remains attached to the pillar on the silicon sample surface. An example of successful bonding chip-to-substrate that survived the destructive shear force testing is shown in cross-section in Figure 4.7. It exhibits very uniform cross-section and no interfaces between the bonded pillar structures. All of the samples tested showed no visible degradation of the organic board materials.

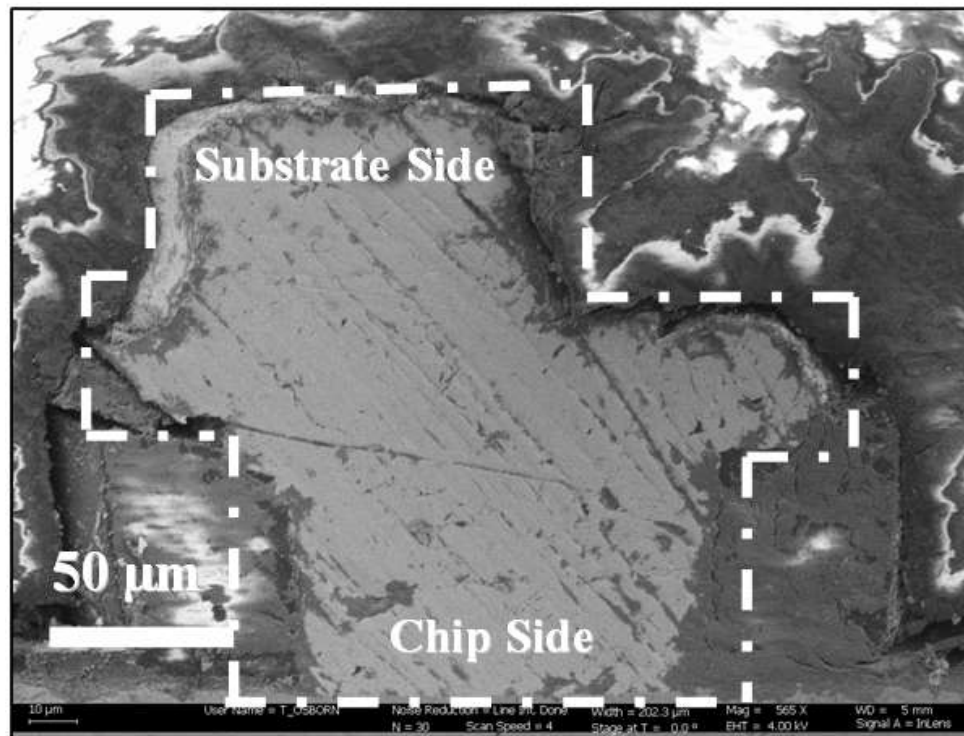


Figure 4.7: SEM cross-section of pillars bonded between Si and FR-4

4.3 Discussion

During the electroless plating process the two copper pillar surfaces grow closer due to the deposition of copper from the electroless bath. As they grow nearer the surfaces begin to conform to one another and terminate plating near one another ($< 1\ \mu\text{m}$) as shown in Figure 4.1. Constant renewal of the copper surfaces during the electroless plating process maintains clean conditions free of oxides and other contaminants. The seam between the surfaces can then be easily rearranged to form a dense copper-to-copper bond without requirements of high temperature or pressure. Unlike copper-copper wafer bonding **Error! Bookmark not defined.**, the required temperature to drive the bonding process is greatly reduced due to the copper surfaces being free of contaminants and oxide. In addition the conformal nature of the electroless plated surfaces to one another provides intimate contact without externally applied pressure. Larger voids in the interface can remain and are minimized using techniques described above. Previously, the surface activated bonding method (SAB) demonstrated that atomically clean copper surfaces readily bond together at room temperature under modest applied pressure.[34,35] This result implies that atomically clean copper readily bonds without an elevated temperature driving force. The necessary temperature for seamless bonding in the all-copper system ($\sim 180^\circ\text{C}$), suggests that the surfaces terminated during the electroless plating process are more readily available to bond than those found in copper-copper wafer bonding [28-33] but less so than those in SAB.[34,35] Therefore, while the surface of the two electrolessly plated regions does have some of the clean and readily bondable character found in SAB, there is still a minimum thermal driving force required. The temperature requirement being $\sim 180^\circ\text{C}$ is in the range typical of many metals for recrystallization and grain growth.[57] The surface chemistry mechanism for this unique, low-temperature bonding process will be investigated further in a future manuscript.

Previously, Nakahara et al and Graebner et al showed that low temperature annealing (100 – 200 °C for 24 hours) of electroless copper films improved the ductility of the film.[58,59] The change in mechanical properties was shown to result from the removal of molecular hydrogen entrapped in the film and recrystallization and grain growth.[58,59] The results shown here agree with this improvement in ductility due to low temperature annealing. The recovery of the ductile nature of copper in the electroless bonded region is important for creating reliable, compliant chip-to-substrate interconnects. However, unlike previous studies, this system is unique in that two distinct electrolessly deposited copper regions are merged during the annealing process. Therefore, the improvement in the mechanical compliance of the all-copper interconnects during annealing comes from three parts, (1) the mixing of the two region interface, (2) the removal of entrapped hydrogen, and (3) recrystallization and grain growth. Therefore, the time and temperature requirements for annealing are based on all three processes occurring.

4.4 Summary

The three components during low temperature annealing that drive the improvement in the microstructure and mechanical properties of the copper-copper bond are: (1) elimination of the bonding interface, (2) hydrogen removal, and (3) recrystallization and grain growth. Annealing at 180°C removed the interface and yielded bond strength of 165 MPa which is 75% of the yield stress of electroplated copper. The plating terminated interface is removed with anneal temperature of 180°C or greater, but remained with annealing at 150°C even with longer anneal times. This showed that there was a minimum temperature barrier to creating a seamless copper-copper bond. The all-copper chip-to-substrate bonding process exhibited superior capabilities compared to solder with respect to both aspects of misalignment (planar and height mismatch). With this process bonding between silicon test chips and organic substrates has been performed

and demonstrated continuous copper connections without any observable degradation of the organic substrate.

CHAPTER 5

DESIGN FOR LOW-K COMPATIBLE ALL-COPPER CONNECTIONS

5.1 Overview

A novel fabrication technique using electroless copper deposition has been used to produce all-copper, chip-to-substrate connections. This process replaces solder by electrolessly joining copper pillars on the chip and substrate. The electroless copper joints were annealed at 180°C after plating. A model was developed to explore methods for lowering the stress within the copper pillar, especially at the point where the pillar intersects the chip surface. The acceptable stress level within the copper pillars is a function of the on-chip dielectric material and the on-chip interconnect structures. In order to avoid fracture of the on-chip dielectric, the stress in the copper pillars should be less than the current lead-free solders that the all-copper pillars would be replacing. A polymer collar surrounding the copper pillars was used to support the pillars and improves thermo-mechanical reliability. The improvement in stress-reduction, ultimately leading to higher reliability, was studied as a function of elastic modulus of the polymer collar support. It has been shown that the pillar stress generated during temperature cycling can be reduced by increasing the modulus of the pillar support and changing the shape of the copper pillars. Finally, three high-contrast photodefinable collar materials were characterized and tested. Nanoindentation experiments were performed to measure the mechanical properties of each material and shear tests were performed to verify the benefits of the higher elastic modulus collars. The work in this chapter was previously published in *Microelectronic Engineering*. [60]

5.2 Review of Previous Modeling and Design Work

The previous work on modeling and design [61] used the adhesive failure of the copper to the chip as the figure of merit for allowable stress, i.e. 148 MPa.[62] This stress level, 148 MPa, is well below the yield stress for copper, but is a concern for the structural integrity of low-k copper interconnects on the die itself. Currently fracture and failure of the brittle low-k dielectric on-chip is becoming an important consideration for flip-chip packaging.

Many approaches have been taken to mitigate stress caused by the coefficient of thermal expansion (CTE) mismatch between silicon and packaging substrates. One compliant interconnect architecture developed by Zhu et al., the G-Helix, has demonstrated high mechanical flexibility.[63,64,16] Kacker et al. showed that consideration of both electrical and mechanical properties are important.[65] The need to protect the on-chip low-k dielectric network was emphasized.[66] While the helix structure is effective in reducing mechanical failure, it is costly due to the multiple step lithography required for fabrication. The two lithography steps required to fabricate the all-copper pillar system could be a more cost effective route to achieve compliant connections, especially since copper pillars are already making their way into commercial products. The fragility for the low-k on-chip networks have also been investigated by Yoon et al.[67] They were able to show that direct attachment applied significant stress to the on-chip interconnects. In addition, they claimed to significantly reduce the stress exerted on the low-k network by using a redistribution layer (RDL) and copper-post style connection.[67]

5.3 Modeling

In the previously reported model, a generalized plane deformation strip (GPD) was used to characterize the design space for copper pillars based on height, diameter, and requirements for both stress and electrical parasitics (L,C).[61] The 3D GPD model considers a slice of the package from the center of the chip along the diagonal. The diagonal slice captures all major components, including a full set of chip-to-substrate connections. The innermost and outermost pillars along the diagonal slice (center and the corner of the chip) reflect the minimum and maximum extremes of thermal deformation. In the GPD model, the nodes on the two sides of the slice are coupled, so that all the nodes in the same plane have identical deformation in the y direction (normal to the surface). This coupling of nodes along the two planes satisfies the generalized plane-deformation constraints. Each plane is neither a free surface nor a true symmetry plane. This boundary restriction has the effect that the slice is free to move as a plane in the y direction, but the surface is required to remain planar. The GPD model is a tradeoff in terms of accuracy and computational complexity, because it uses an assumed boundary condition instead of the symmetry boundary conditions. The GPD model showed that for a given pillar height and diameter (i.e. 50 μm diameter and 500 μm height), surrounding the pillar with a polymer collar reduced the stress experienced by the copper pillar. Furthermore, as the elastic modulus of the polymer collar increased, the stress on the pillar was further reduced, as shown in Figure 5.1.[61]

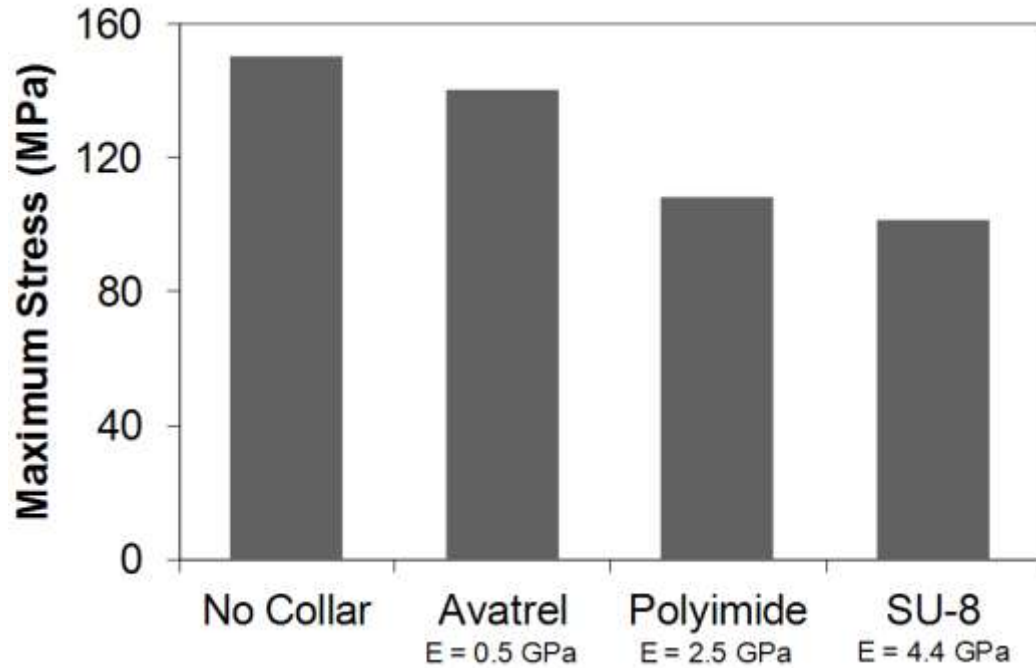


Figure 5.1: Results from the GPD model previously developed showing the benefits of polymer collar supports for copper pillars

In order to further analyze the benefits of surrounding the copper pillar with a polymer collar, a new model was created. A single copper pillar was modeled for simplicity and rapid computation, as shown in Figure 5.2. The single pillar is intended to represent the chip-to-substrate connection which experiences the maximum stress during thermal expansion due to the CTE mismatch between FR-4 and silicon. It represents the position farthest from the neutral point, as shown in Figure 5.2. Utilizing boundary conditions to mimic the previously modeled GPD results for a collar-free copper pillar, the model successfully replicates the GPD results of maximum stress felt by the copper pillar for each of the three previously studied polymer collar systems (Avatrel, Polyimide, and SU-8). The geometry and material properties used for the model are summarized in Tables 5.1 and 5.2. Since the single pillar model allows for rapid computation, many permutations of the polymer collar were investigated. In this report COMSOL Multiphysics was used to compute the finite element model. In COMSOL the boundary

conditions were set to emulate the GPD model. Two sides of the model were held planar. Next, one edge at the base of the model was fixed to prevent free body movements. Finally, the last side of the model was forced to expand related to the CTE mismatch of silicon and FR-4. The precise values of these conditions were optimized until the results of the previous GPD model could be correctly predicted with the single pillar model. The final values for these two boundary conditions were: 1.25×10^{-6} for FR-4 and 0.15×10^{-6} for Si. The number of elements in the model varied based on the geometry used, but a typical value was approximately 20,000. On a desktop computer with 4 GB of RAM, each solution required approximately 5-10 minutes.

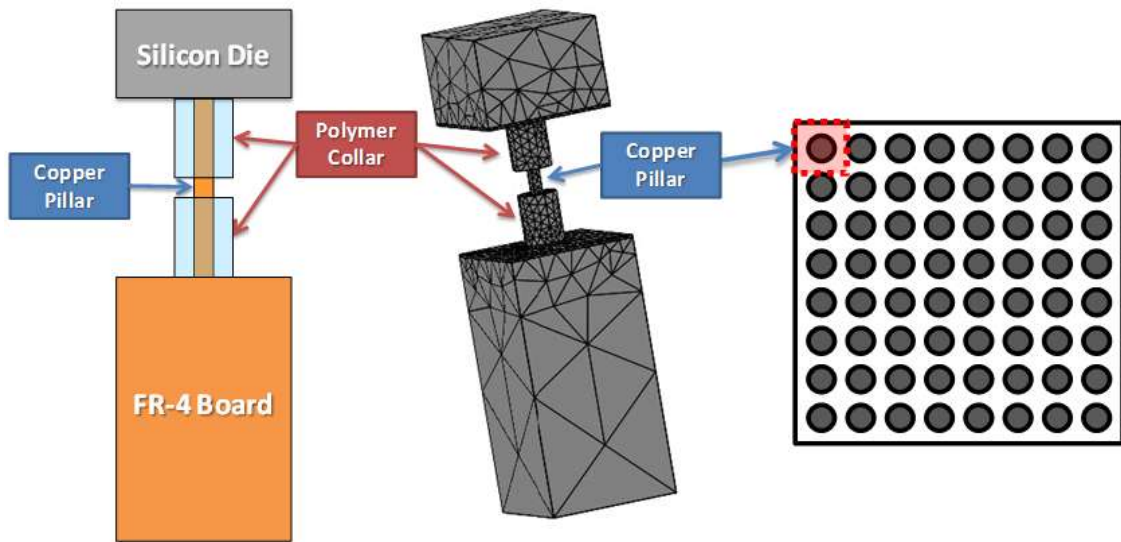


Figure 5.2: Illustration and finite element model of the single copper pillar system used in this study

The objective of the modeling work was to examine approaches to lowering the stress exerted by the copper pillar on the die. This is intended to minimize the risk of failure in the on-chip low-k copper interconnect network. The metric chosen as an acceptable level of stress was that of the yield stress for currently used solder alloys in flip-chip packaging, such as $\text{SnAg}_{3.5}\text{Cu}_{0.7}$. The yield stress of $\text{SnAg}_{3.5}\text{Cu}_{0.7}$ is highly

dependent on the strain rate and temperature.[68,69] Therefore, an intermediate value of 45 MPa was chosen as the no-lead target in this work. In addition, a low stress target of 30 MPa for eutectic SnPb solder was chosen.[70]

Table 5.1: Mechanical properties used in the model

Mechanical Properties		
Material	E (GPa)	γ
Si	131	0.27
FR4	22	0.28
Cu	110	0.35
Au	83	0.44
Polymers	Variable	0.33

Table 5.2: Dimensions of the modeled geometry

Dimensions of Geometry (in μm)	
Chip	500 x 500 x 350
Substrate	500 x 500 x 1000
Cu Pillar	D = 50, H = 500
Polymer Collar (x 2)	ID = 50, OD = 100, H = 200

To reduce the stress exerted on the chip surface due to the rigidity of the copper pillar, the effect of increasing the elastic modulus of the polymer collar and lowering the modulus of the pillar itself was tested. The modulus of the pillar was lowered by comparing copper to gold. Figure 5.3 shows these two sets of comparison. The maximum stress observed in the copper pillar decreased with increasing polymer collar modulus until the modulus reached approximately 8.25 GPa for a copper pillar and approximately 6.5 GPa for a gold pillar. For the copper pillar, this results in a maximum

stress of 78.4 MPa within the copper pillar. This is a dramatic reduction from the collar-free case which has a maximum stress of 148 MPa. Additionally, Figure 3 shows that as the polymer collar modulus increases beyond 8.25 GPa, the maximum stress within the copper pillar increases. As the collar modulus increases above 8.25 GPa, the location of maximum stress within the copper pillar shifts from the chip-pillar interface toward the center of the copper pillar. This shift in stress along the length of pillar is illustrated in Figure 5.4. This observation is important because fracture of the on-chip low-k dielectric is initiated by stress at the chip-pillar interface. Thus, the 45 MPa goal refers to the chip-pillar interface, regardless of the stress elsewhere in the pillar as long as the pillar does not yield in other locations. Copper is not likely to yield under any conditions considered here because it has a very high yield stress, ~225 MPa.[55] Increasing the modulus beyond 8.25 GPa in practice would be very difficult since it places an ever higher burden on the photosensitive polymer collar, including high contrast, fracture toughness, and high modulus.

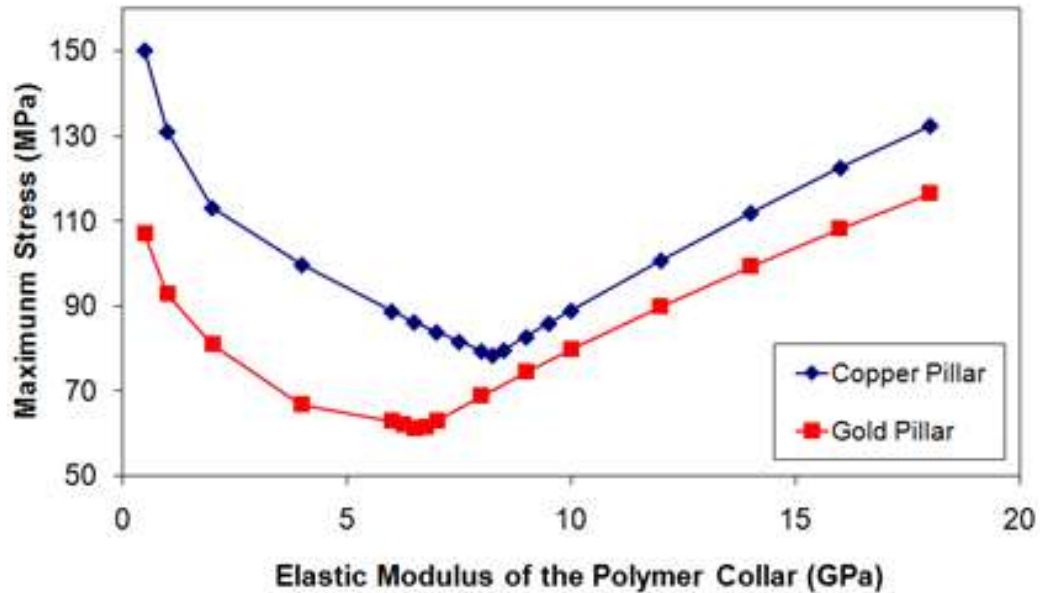


Figure 5.3: Plot of the maximum stress in the pillar as a function of the elastic modulus of the polymer collar supports

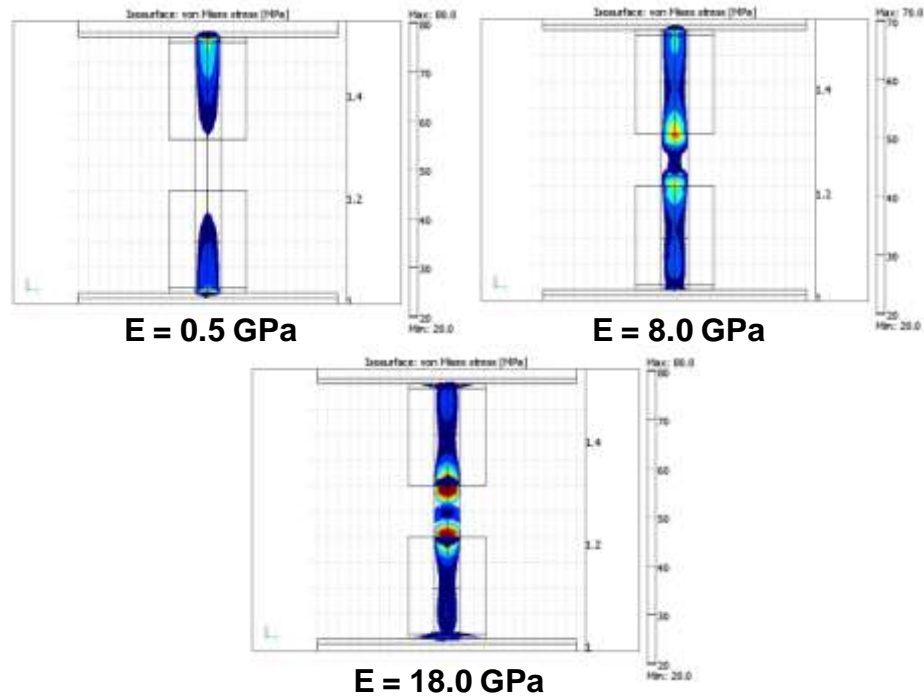


Figure 5.4: Isosurface plots illustrating the shift in the location of the maximum stress from the pillar-to-chip and pillar-to-substrate interfaces into the center portion of the pillar as the elastic modulus of the polymer collar increases

Shifting the high-stress point in the copper pillar away from the chip-pillar interface is an effective tool for lowering the impact on the on-chip, low-k dielectric. A multi-level collar structure can be considered since the collar constraints are considerable, as mentioned above. First, a bi-layer collar was considered where the first layer, closest to the chip, had a higher modulus than the second layer, which was thicker, as illustrated in Figure 5.5. This approach separates the collar functions into two areas: the first layer is thin and has a very high modulus (but need not be photosensitive), and the second layer is photosensitive with high contrast. Therefore, it would be advantageous to limit the thickness of the high modulus material, and then complete the collar with a material that has superior photo-processing capabilities such as Avatrel 8000P or SU-8. For this

model, a 10 μm thick, high-modulus collar was placed at both the chip-pillar and substrate-pillar surfaces. Then, the remaining 190 μm of collar material was modeled using known materials capable of forming high aspect ratio structures with $E_{\text{top}} = 2.5 \text{ GPa}$ and $E_{\text{top}} = 4.0 \text{ GPa}$ respectively.

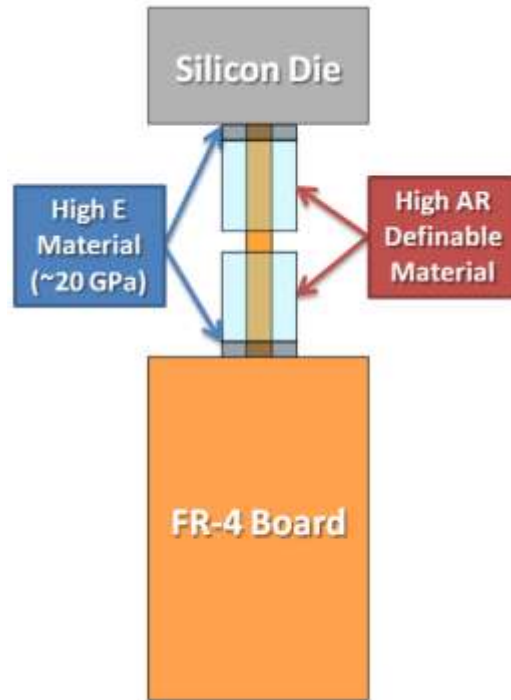


Figure 5.5: Illustration of the concept of the bi-layer collar support structure

Based on this “bi-layer” collar, the overall maximum stress (anywhere within the copper pillar) can be further reduced below that of a single collar material, as shown in Figure 5.6. While the single material collar has four stress concentration points along the length of the pillar (at the collar-chip, collar-substrate, and where the collar ends near the middle of the pillar), the bi-layer structure has six stress concentration points. The additional two are at the interface between the two collar materials. These additional two stress concentration points serve to redistribute the stress to more locations along the length of the pillar and result in a lower stress level at the chip-pillar interface. The

minimum in stress was found to be 58.1 MPa and 52.8 MPa for the $E_{\text{top}} = 2.5$ GPa and $E_{\text{top}} = 4.0$ GPa top layer collar systems respectively. These minima in stress are found using bottom layer collar with elastic moduli of 21 GPa ($E_{\text{top}} = 2.5$ GPa) and 22 GPa ($E_{\text{top}} = 4.0$ GPa). By utilizing the “stiff” base collar approach the stress on the chip surface was reduced by approximately 47% in each case, compared to a single collar comprised of the top collar material.

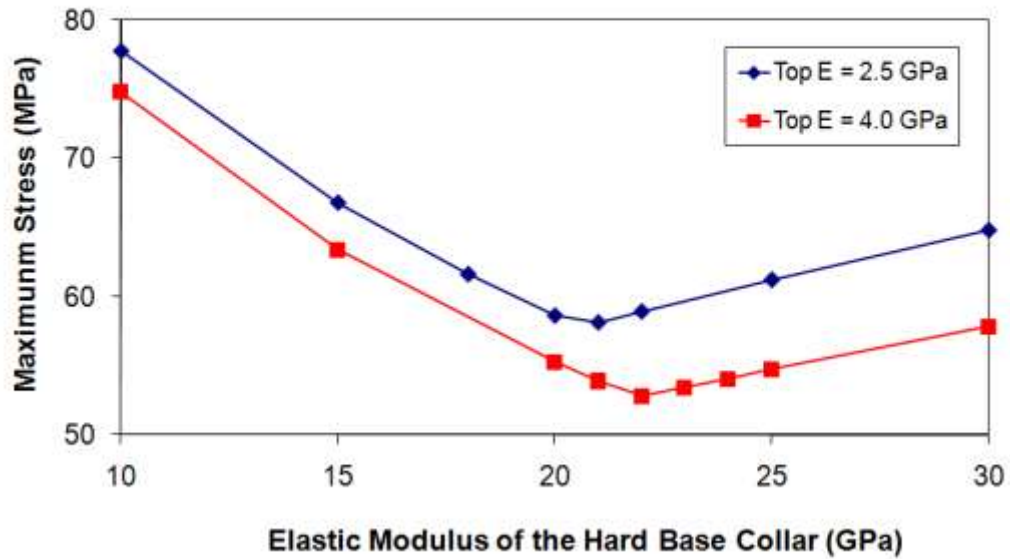


Figure 5.6: Plot of the maximum stress in the pillar as a function of the hard base collar modulus with two different top collar materials

One of the most useful aspects of the all-copper connection is that the geometry of the pillar is only limited by the photolithography process. Since there is no solder reflow, the shapes that are electroplated remain unaltered upon bonding. Utilizing this capability there is no longer a restriction to either spherical (solder balls) or cylindrical (pillar) geometries. In fact, there are likely to be other geometries that more effectively dissipate

stress. Further reductions in stress at the chip-pillar interface can be achieved by considering the in-plane stress distribution at the chip-pillar interface.

Analysis of the in-plane stress distribution at the chip-pillar interface shows that the highest points in stress are the leading and trailing edge of the pillar (along the direction of thermal expansion). That is, as the chip and substrate thermally expand at different rates, the pillar is placed in compression at one side of the pillar, and tension at the other side. The pillar exerts very low stress at positions not in the direction of expansion because there is little strain in those directions. Thus, one can consider geometries other than cylindrical in order to distribute a given force (dictated by the CTE mismatch between Si and FR-4) over a wider area (lower effective stress at the critical point in the chip-pillar interface).

Expanding the effective surface area of the pillar in the direction of the thermal expansion was achieved by considering an elliptical pillar. Using the ellipse requires careful consideration of the orientation of the I/O so that the broader face of the elliptical pillar is facing the direction of thermal expansion. Three different elliptical shapes were chosen based on their eccentricity. For simplicity, the ratio of the two diameters that define the ellipse, A and B, will be used to define the shape, as shown in Figure 5.7. While holding the cross-sectional area approximately constant, three different A/B ratios were chosen and compared to the 50 μm diameter circular pillar. Cross-sectional plots of the stress at the chip surface for a cylinder with $A/B = 1$ and an ellipse with $A/B = 3$ are also shown in Figure 5.7 to demonstrate the reduction in stress due to the larger area the ellipse presents normal to the direction of thermal expansion. The parameters defining the ellipses studied are summarized in Table 5.3.

Table 5.3: Dimensions used for the elliptical I/O modeling

Elliptical I/O Dimensions (μm)		
A	B	A/B
50	50	1
60	40	1.5
90	30	3
125	20	6.25

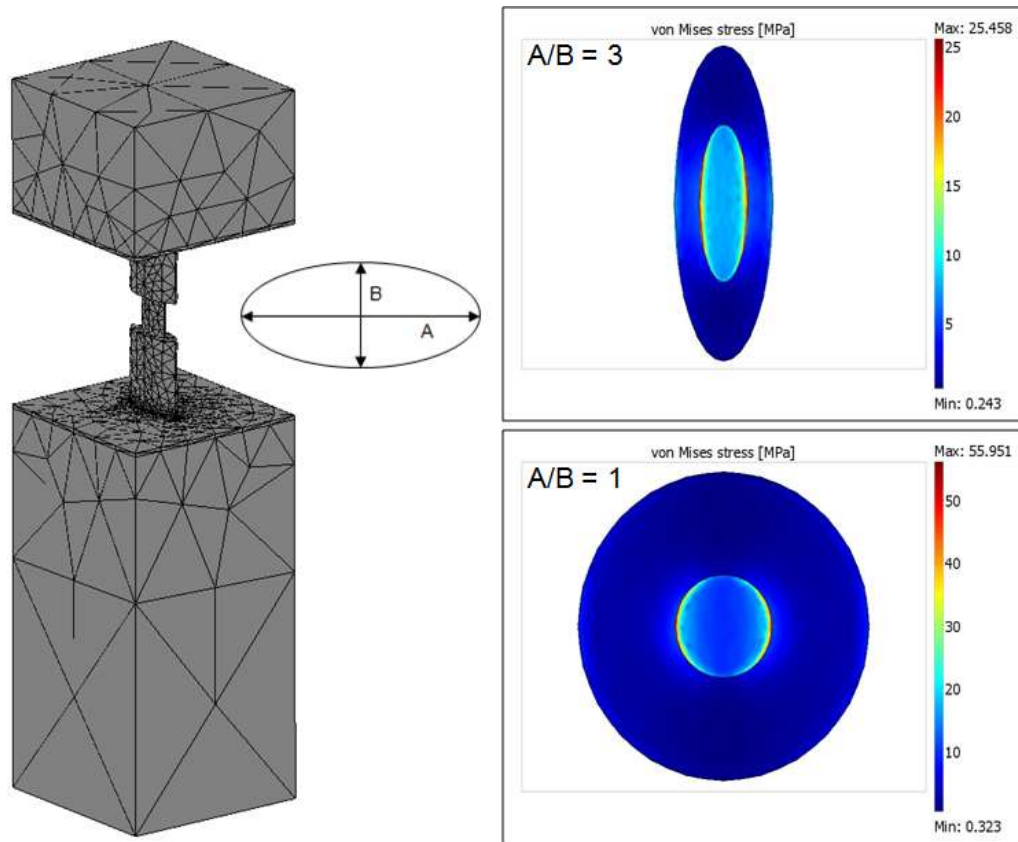


Figure 5.7: FEM model of the elliptical pillar, definition of the parameters A and B, and stress plots demonstrating the effect of the elliptical shape on reducing stress on the chip surface compared to a circular cylinder

The elliptical pillar simulations used the previously discussed optimized bi-layer collar structures. The elastic modulus of the thin, first layer of the collar was 21 GPa and the elastic modulus of the thicker, second layer of the collar was 2.5 GPa. The benefits of the elliptical pillar are shown in Figure 5.8. As the pillar A/B ratio is increased, the overall stress is dramatically reduced. In addition, the chip surface stress, which is of primary interest, is reduced even further for each increase in A/B. The elliptical pillar demonstrates that increasing the area over which the force is applied lowers the thermal stress at the most critical chip-pillar location. The elliptical front to the pillar decreases the overall maximum stress in the structure and decreases the maximum stress found at the chip surface. Utilizing the ellipse geometry, the stress target of 45 MPa is achieved at an A/B ratio of ~ 1.5 , for both overall maximum stress and chip surface stress.

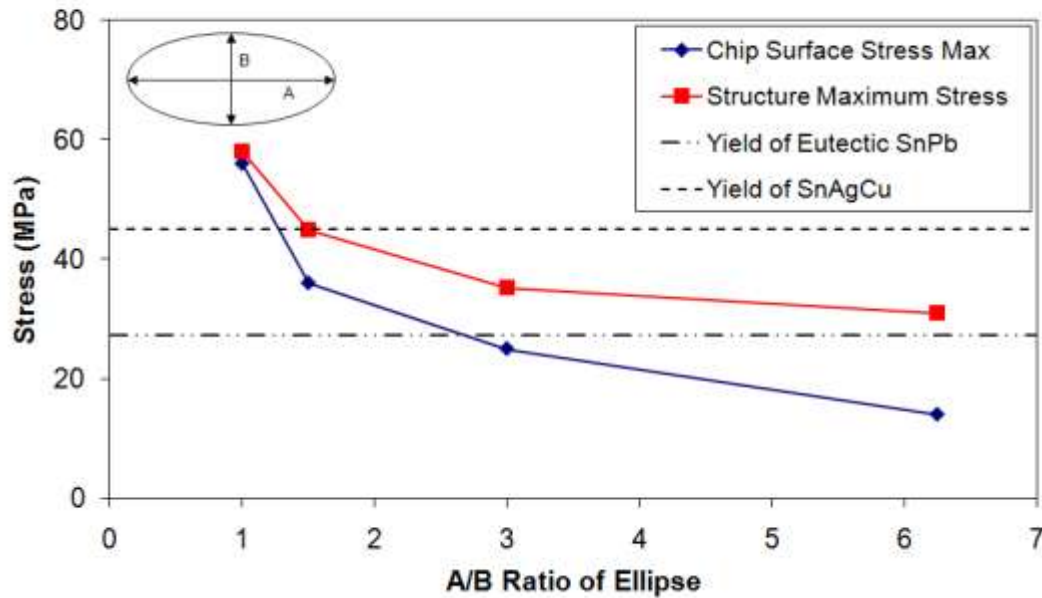


Figure 5.8: Plot of the maximum stress as a function of the A/B ratio of the pillar

It is important to note that as the A/B ratio increases, the maximum stress at the chip surface and the maximum overall stress in the structure diverge in value. The divergence implies that as the structure becomes more elliptical in nature, the stress is dissipated over a broader portion of the pillar, and is no longer concentrated near the ends. In the previously studied cylindrical case, the stress concentrates at the chip-pillar and pillar-substrate interfaces and therefore the values of overall maximum stress and the maximum found at the chip surface coincided. With the elliptical pillar, the maximum stress is no longer found at the chip-pillar interface, implying a distribution of the stress across a broader portion of the pillar.

Another challenge is obtaining materials for the collar. A high modulus first layer dielectric is desired. If the elastic modulus of the base collar is allowed to change from the cylindrically optimized case of 21 GPa, then a critical modulus value can be found for each A/B ratio that still satisfies the required maximum chip surface stress of 45 MPa. In fact 21 GPa could be a very difficult value to achieve for any organic based polymer system. Knowing specifically what elastic modulus is required for each given A/B ratio to achieve the necessary reduction in stress below 45 MPa at the chip surface is valuable for practical implementation. Figure 5.9 shows the critical modulus to achieve the required maximum chip surface stress of 45 MPa as a function of the A/B ratio of the pillar. As the A/B ratio increases the required modulus for the hard base is reduced rapidly. At $A/B = 3$ the required modulus is below 5 GPa, which is readily obtainable using polymer systems such as polyimides.

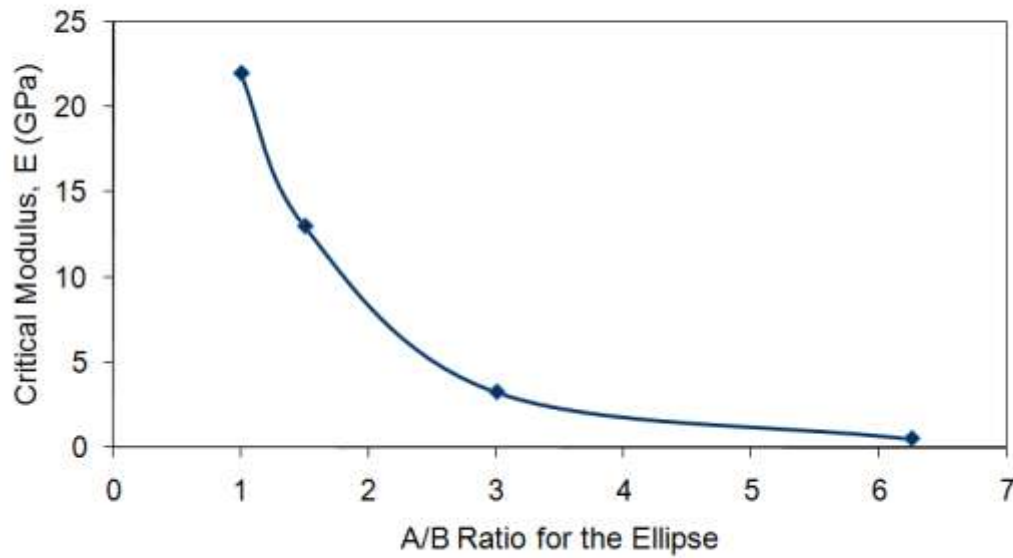


Figure 5.9: Plot of the modulus needed for the base collar for each given A/B ratio to satisfy the chip surface stress requirement of 45 MPa

5.4 Experimental Results

In order to validate the modeled results, three different polymer collar materials were tested experimentally. Feng et al. have shown that processing conditions, such as curing temperature, can have a dramatic impact on mechanical properties of SU-8.[71] Therefore, the modulus of each system used was experimentally measured in order to correctly compare the shear testing results. The results from the nanoindentation testing are given in Figure 5.10. Avatrel 2195P is the softest material ($E = 1.0$ GPa, $H = 0.1$ GPa). SU-8 and Avatrel 8000P had similar values for reduced modulus (SU-8 $E = 3.3$ GPa, Avatrel 8000P $E = 3.1$ GPa), and different hardness values (SU-8 $H = 0.3$ GPa, Avatrel 8000P $H = 0.2$ GPa). The difference in hardness is important because brittle

failure may occur. SU-8 has been shown to be very brittle even after post exposure bake.[71] Avatrel 8000P is not as brittle as SU-8 due to its long-chain hydrocarbon backbone and lower cross-link density.

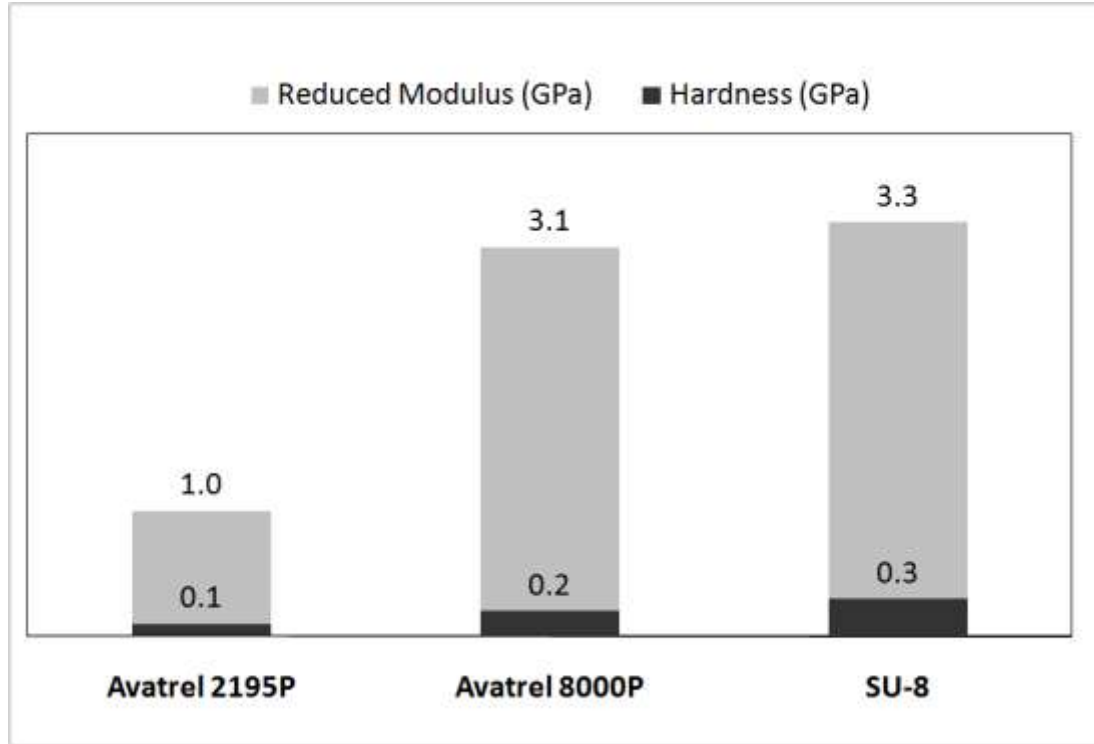


Figure 5.10: Summary of nanoindentation results for the three materials for modulus and hardness

Shear testing of bonded copper pillars with each collar system was performed. The results of these tests are summarized in Table 5.4. The three different systems tested sheared at 11.4, 13.2, and 24.5 N for the Avatrel 2195P, SU-8, and Avatrel 8000P collar cases respectively. The higher elastic modulus collar materials yielded higher shear force to rupture the copper pillars compared to the conventional Avatrel 2195P. In all cases the point of rupture was located at the pillar-to-substrate interface. This implies that the copper-copper joint was sufficiently strong to withstand the forces applied in all three cases. However, the significant increase in shear force to break for Avatrel 8000P over

SU-8 is not only due to elastic properties. The values found for shear testing Avatrel 2195P collars compared with those made of Avatrel 8000P are more consistent with the model predicted benefit in stress dissipation. The higher shear stress values of Avatrel 8000P collars compared to SU-8 was due to its higher fracture toughness. The more brittle nature of SU-8 leads to brittle fracture without plastic deformation. This result also demonstrates the benefit of the Avatrel 8000P collar samples having a unit increase in aspect ratio versus the Avatrel 2195P or SU-8 collared pillars.

Table 5.4: Shear testing results for the three different collar materials

	Shear Force to Break (N)	Aspect Ratio (H:D)
Avatrel 2195P	11.4	2
SU-8	13.2	2
Avatrel 8000P	24.5	3

Based on the previously the modeled results this increase in aspect ratio can have a dramatic impact on the flexibility of the interconnect.[61] Therefore, future work should be focused not only on fabrication of the optimum collar material structure but also achieving as high aspect ratio as possible. The need for high aspect ratio further supports the need for a two layer collar approach, owing to the typically limited photo-definability of exceptionally hard polymer materials.

5.5 Summary

In this work, a model was created to study the benefits of the polymer collar surrounding the copper pillar chip-to-substrate interconnect. The target for stress reduction on the chip surface, less than 45 MPa, was achieved using an elliptical pillar with an optimized bi-layer collar structure. This optimized approach allows the all-copper interconnect architecture to be compliant with fragile low-k on-chip interconnect networks. Experimental verification of the benefits of the higher elastic modulus polymer collar was performed.

CHAPTER 6

FUNDAMENTALS OF THE ALL-COPPER PROCESS

6.1 Overview

The all-copper process creates solid copper connections using electroless deposition followed by low temperature annealing. Understanding when the first bonds are formed and how they grow and evolve during the bonding process is key to understanding the fundamental mechanisms of bonding. In order to investigate what takes place during the deposition process and if bonds were formed prior to annealing, electrical characterization of the deposition was performed. It was found that electrically conductive bonds were formed by electroless deposition without annealing. The resistance of these bonds was then reduced by an order of magnitude with annealing. This implies that some areas between the electroless deposits bond during deposition, but they are not mechanically stable and have been shown previously to be fragile. Once annealing takes place, the bonded area increases via the ‘knitting’ process as seen in cross-sections as the removal of the seam between the plated regions.

In addition, the process is performed using electroless gold deposition and annealing to validate that the process is not unique to the electroless copper bath chemistry or to copper the metal itself. Gold bonding is demonstrated with plating and annealing at 180 C for 1 hr. In the process of this test, homemade electroless baths were created for depositing a palladium catalyst layer and gold itself.

The electrical characterization portion of this chapter has been submitted for publication in the Journal of the Electrochemical Society.[72]

6.2 Electrical Characterization of Bonding

A better understanding of the original electroless copper deposition and bonding process was needed to move forward and improve the process. Therefore, several experiments were performed to characterize what contributes to the unique capability of the process to form fused copper-to-copper bonds at moderate temperatures. The first question to investigate was to what extent bonds are formed between the two growing copper pillar surfaces during the electroless deposition process. Copper parallel line capacitors were micro-fabricated to measure the electrical resistance between two copper portions as they grow together via the electroless copper deposition process. In essence this test was used to verify the presence of electrically conductive bonds forming during the deposition, and to what extent the annealing process improves this bond.

Using a four-point probe technique, the resistance between the isolated lines of the capacitor was measured while the sample was immersed in the electroless copper plating bath. Since the electrolyte has ionic conductivity the resistance is measurable but large in comparison to metallic bonds. An illustration of the equivalent circuit for this system is shown in Figure 6.1. Therefore, the resistance is a useful metrology to track the progress of the plating. Measurements of the resistance versus time of deposition are shown in the plot in Figure 6.2. As the deposition progresses the resistance slowly reduces. Once the deposition is completed, and no anneal is applied, the resistance is dramatically reduced. This implies that metallic copper-to-copper bonds are indeed formed via the deposition process. Enhancement of the bonds takes place during the moderate temperature anneal process. Figure 6.3 shows three levels of magnification of a typical sample after completing the electroless deposition. Under the highest magnification, intimate contact between portions of the two samples is observed. The resistance measured after plating is reported in Table 6.1 for three typical samples.

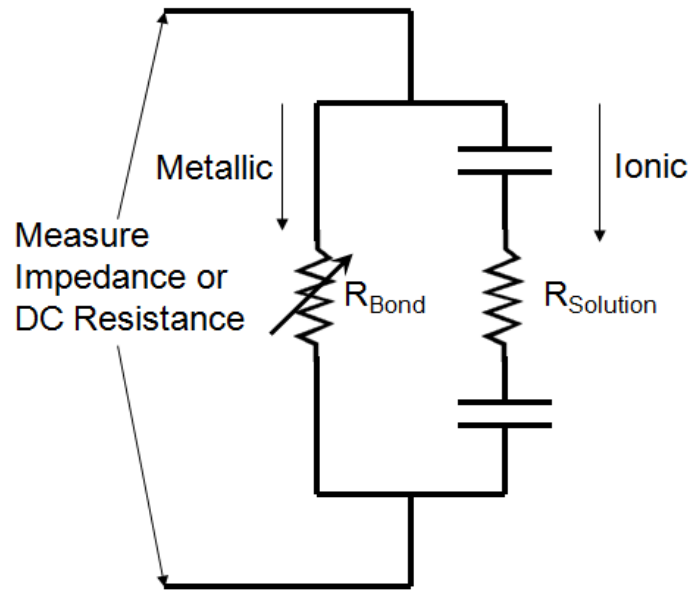


Figure 6.1: Equivalent circuit for the electroless deposition process

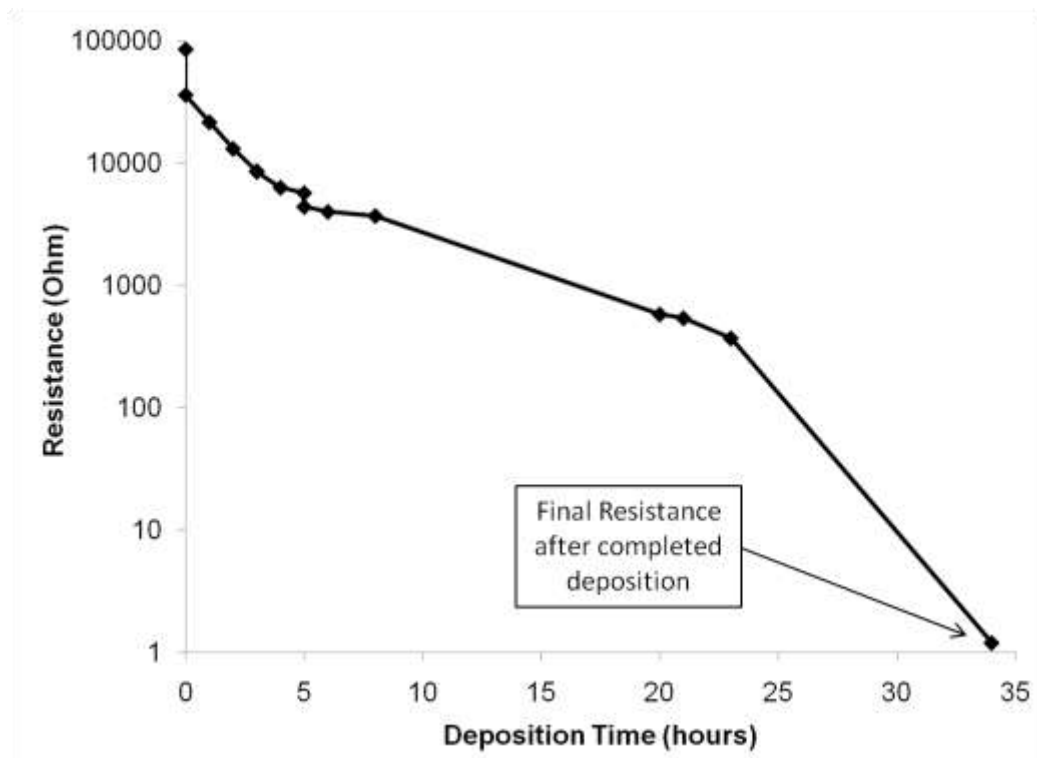


Figure 6.2: Plot of the resistance measured between the copper lines as a function of electroless deposition time

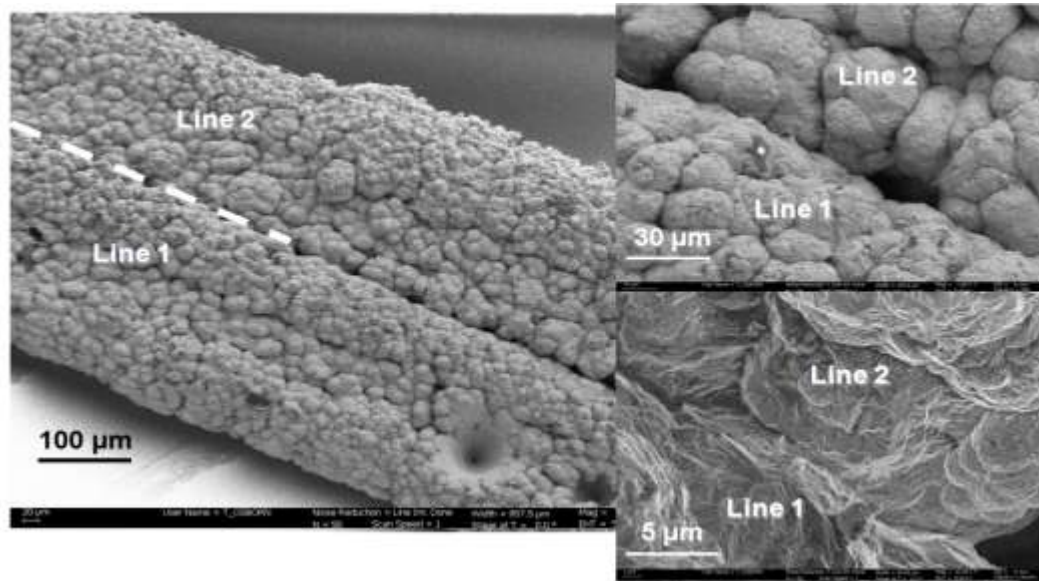


Figure 6.3: SEM images of the bond between lines after the electroless deposition

Table 6.1: Measured resistance of the bonded copper lines before annealing and after annealing at 180 C for 1 hour in nitrogen ambient

Sample	Resistance Prior to Annealing (mΩ)	Resistance After Annealing at 180 C, 1 hour (mΩ)
1	5.8	0.7
2	2.5	0.2
3	3.8	0.5

Once the samples were plated to form metallic bonds, they were annealed at 180 C for 1 hour in nitrogen ambient. After anneal the resistance was measured again and found to reduce by about an order of magnitude in all three cases, as reported in Table 6.1. This supports the concept of the bonds recrystallizing during the anneal process and also growing in surface area via the ‘knitting’ process to remove any interfaces or seams.[54] Metallic bonds being formed at room temperature are promising for future process optimization. It implies that given proper deposition conditions a process that no longer requires elevated temperature annealing to remove seams between the electroless plated regions could be developed. In fact, this is essentially what the ‘superfilling’ process at the nanoscale does in damascene trenches.

6.2 Electroless Gold Deposition and Bonding

The second analysis used was to attempt the bonding process with an alternative material. This was used to exclude the possibility that the process succeeds only because of properties unique either to the electroless copper plating and/or the deposited copper itself. The material chosen for comparison was gold. Since electroless deposition baths for gold are known [51], it was a logical choice for comparison.

Electroless deposition for gold requires is more difficult than copper, since the gold-cyanide complex is very strong, a stronger reducing agent is required, hydrazine. In addition, the reactions will not take place on poor catalyst surfaces at any appreciable rate. This means that using previously fabricated copper pillars is not possible without depositing a suitable catalyst layer prior to the electroless gold process. Palladium is an excellent catalyst for the hydrazine oxidation reaction and therefore was chosen to catalytically activate the copper pillar surfaces before gold deposition. In another laboratory study an in-house electroless platinum deposition bath was developed [52], and it was a logical extension to create an electroless bath for palladium to coat the

copper pillar surfaces. The compositions for both the electroless palladium and electroless gold baths used in this study were given previously in Table 3.2.

After coating copper pillars with a thin layer of palladium, samples were flip-chip aligned and immersed in the electroless gold bath. Once gold deposition was completed the samples were annealed at 180 C for 1 hr. After annealing they were broken apart and analyzed for bonded pillar pairs. Figure 6.3 shows an SEM image of the gold-gold bonding region between two pillars. The image has an EDS elemental mapping overlay to illustrate the different areas of the two copper pillars (red) and the gold joint region (green).

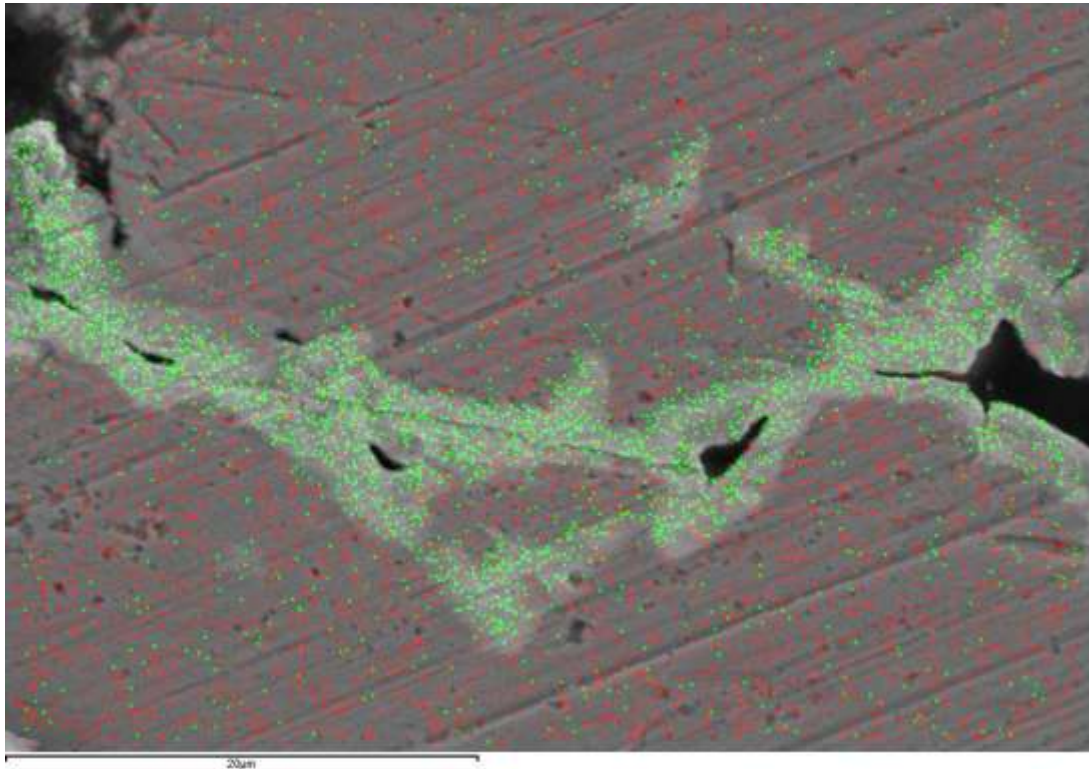


Figure 6.4: SEM/EDS image of a gold-gold bond formed between copper pillars by electroless gold deposition and annealing (green = gold, red = copper)

The success of the gold deposition and bonding is proof that this process is not unique to copper plating or metallurgy. However, copper is still the most desirable material for this process based on cost, electrical performance, and material matching to both the copper pads on the die and the copper traces on the package.

6.3 Summary

In this chapter, fundamentals of the all-copper process were studied. It was shown from electrical measurements that conductive bonds are formed during the deposition process. Annealing reduced the resistance of the bonds significantly and allows recovery of mechanical properties. Formation of electrically conductive bonds during plating supports the concept of creating seamless copper-to-copper bonds during deposition and no longer requiring annealing to remove the interface in the joint. Annealing may still be required in some fashion to promote recrystallization and grain growth to recover mechanical strength in the deposited copper. In the second set of experiments, gold-gold bonding was successfully demonstrated. Bonding with an all-gold process removes the possibility of a unique property of the electroless copper bath or the copper metal itself as being the reason bonds are formed at low temperature. The conclusions that both tests support is that by electrolessly depositing the metal in the joint, true metal-metal bonds are formed. Then during annealing these bonds serve as starting points for the ‘knitting’ process to initiate. Once the ‘knitting’ is initiated at the bonds, it propagates through the entire interface and closes the seam to form a solid metal connection. At the same time, recrystallization, grain growth, and the release of entrapped hydrogen from the electrolessly plated copper are all contributing to improve the mechanical properties of the joined region. Without the recovered ductility of the plated joint, closing the seam alone may not have been sufficient for mechanical stability.

CHAPTER 7

IMPROVED ELECTROLESS DEPOSITION VIA POLYETHYLENE GLYCOL SUPPRESSION

7.1 Overview

A novel fabrication technique using electroless copper deposition has been used to produce all-copper, chip-to-substrate connections. This process replaces solder by electrolessly joining copper pillars on the chip and substrate. Previously, successful solid copper-to-copper bonding was demonstrated using a standard electroless copper bath followed by low-temperature annealing at 180 C for 1 hour in a nitrogen environment. However, this process was not considered to be viable for industrial use due to the inherently slow deposition using the additive free bath at room temperature. In fact, deposition typically required approximately 18 hours to complete. Therefore, an approach utilizing elevated temperature combined with polyethylene glycol (PEG) based deposition suppression has been developed. By increasing the temperature the transport of reactants and products in and out of the deposition site is increased, but the addition of PEG to the bath allows for some degree of deposition rate control. This situation allows for a kinetically controlled deposition process to take place while still maintaining good quality copper deposits without significant porosity or voiding. A reduced plating time of 2 hours with 1 ppm of PEG added to the bath has been demonstrated. The increased deposition rate led to a reduced interface between the growing copper portions, and fused to create mechanically stable bonds using an 180 C 1 hour anneal process. The work in this chapter has been submitted to the Journal of the Electrochemical Society.[72]

7.2 Motivation for PEG deposition process

Previously, an electroless copper plating process followed by low-temperature annealing that creates copper-to-copper bonds between chip and substrate was shown.[61] The process shows some promise as a first-level packaging solution for many reasons. It does not require cost-prohibitive materials or processes. There have been several reports related to gold-gold thermo-compression or thermo-sonic bonding as a potential solder-free solution.[36,38,39] Unfortunately the cost of gold and the creation of new metallurgical joints (i.e. not an all-copper interconnect structure) are potentially problematic.

The all-copper chip-to-substrate electroless process has been shown to be able to correct for in-plane and through-plane mismatches, similar to solder [61]. However, one severe disadvantage was the slow electroless deposition process (e.g. up to 18 hours of plating time).[61] Previous attempts to speed up the plating process by using higher temperature baths were unsuccessful, resulting in poor quality copper and insufficient chip-to-substrate bonding.

The scope of this work in this chapter is to reduce the electroless plating time from the previous value of 18 hours. It is desirable to have a kinetically limited deposition process so that plating in small crevices between the copper pillars will occur uniformly across the package and across each pillar set. To accomplish this, an elevated temperature electroless bath was used, so that mass transfer is sufficient, along with suppression of the plating by addition of polyethylene glycol (PEG).

The effects of PEG, sulfopropyl sulfonate (SPS), and other additives on the electroless copper deposition process have been reported extensively.[73-79] Electroless copper plating has been shown to exhibit ‘superfilling’ behavior analogous to the acid copper electroplating damascene process [80] using PEG as the only additive [73]. The ability to plate in the highly restricted space between pillars was an important aspect of the previous publication.[61] As plating occurs on the two pillars and the gap between

them closes, it is very important that the two plating fronts merge together as much as possible. The merging of the copper pillars may be similar to seamless filling of the center of a through-hole or other restricted structure where plating occurs on the side-walls and a solid fillet is obtained with voids. Dow et al. have demonstrated such a seamless filling of a through-hole by using a specific additive in the copper bath.[81] They demonstrated that additive chemistry can have a significant impact on the deposition profile over scales much closer to that used in this work (10-100 μm), versus the nanoscale trenches which are used to test damascene plating (100 nm) applications. The goal of this work is to significantly increase the electroless deposition rate between the merging copper pillars and retain the voidless, intimate contact obtained between the joined copper pillars.[61]

7.3 Results

The goal of this work was to reduce the plating time required for complete pillar-to-pillar bonding. Previously, long time periods were devoted to the room temperature electroless deposition process, typically 18 hours.[61] Increasing the temperature did increase the plating rate, however, the deposit was porous and unacceptable. In general, there are fewer parameters to manipulate in electroless deposition, compared to electrodeposition, because current and potential cannot be externally controlled. The temperature of the electroless bath was first increased resulting in higher deposition rates. In fact, it is common to use electroless copper processes 45°C to 65°C. Unfortunately, the transport of reactants and products into the small seams between copper pillars is different from open-surface plating applications. Figure 7.1 illustrates the multi-scale, highly constricted system for pillar-to-pillar plating.

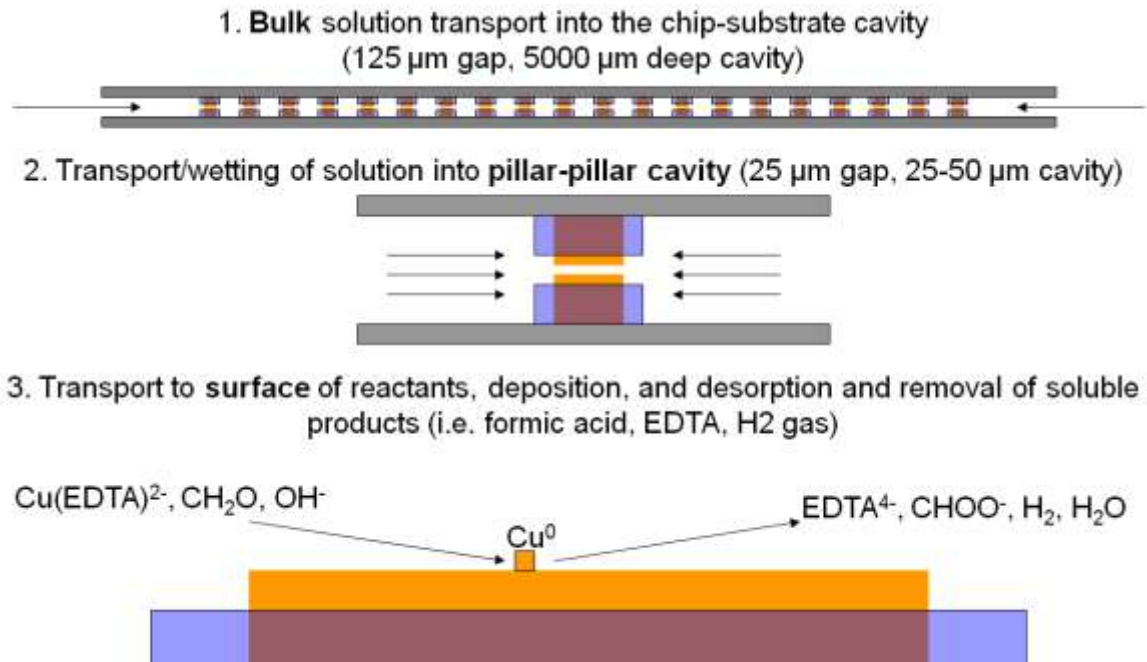
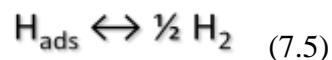
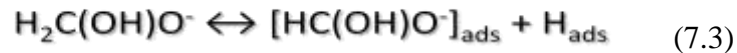
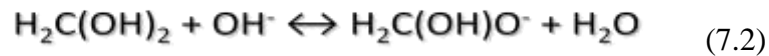
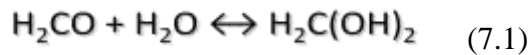


Figure 7.1: Concept of the multi-scale transport challenges in the all-copper process

The difficulty in removing products is particularly important since the reducing agent, formaldehyde, generates hydrogen gas as a by-product which can form bubbles between the pillars. The anodic reactions taking place on the copper surface include the hydrolysis of formaldehyde, Equation 7.1, dissociation of methylene glycol, Equation 7.2, dissociative adsorption, Equation 7.3, charge transfer, Equation 7.4, and desorption of hydrogen, 7.5.[82]



If the transport of hydrogen from the surface is inadequate, gas entrapment within the spatially restricted seam can occur and lead to significant porosity in the plated metal. Figure 7.2 shows SEM images of the results obtained from elevated temperature plating experiments using the additive-free electroless bath. The samples plated at 45°C and 65°C both showed significant porosity in the bond region. After annealing, the copper pillars were not mechanically bonded or stable.

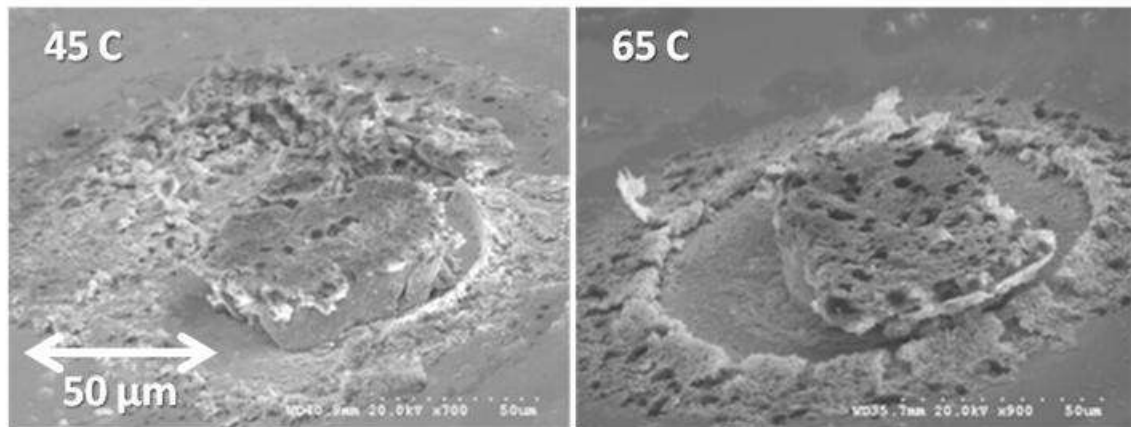


Figure 7.2: SEM images of results from attempting to plate at elevated temperature without additives in the bath (left) 45 C (right) 65 C

Since increasing the temperature alone leads to transport limitations and porosity, an additive based strategy was employed. If the temperature could be increased, but the deposition rate suppressed by adsorption of an inhibitor, the kinetically controlled conditions could be maintained. PEG was chosen as an inhibiting additive since its interactions with copper surfaces and electroless plating chemistries have been studied.[73-79]

In order to characterize the effects of PEG on our electroless plating rate, various concentrations of PEG were used and the plating rate was measured. Clean copper

surfaces were used for this experiment to reduce the transport limitations as much as possible. The deposition temperature was chosen to be fixed at 70°C. Figure 7.3 shows the results of the plating rate tests. The plating rate was dramatically reduced with only a few parts per million (ppm) PEG in the bath. In fact, at 4 ppm the plating rate is near zero.

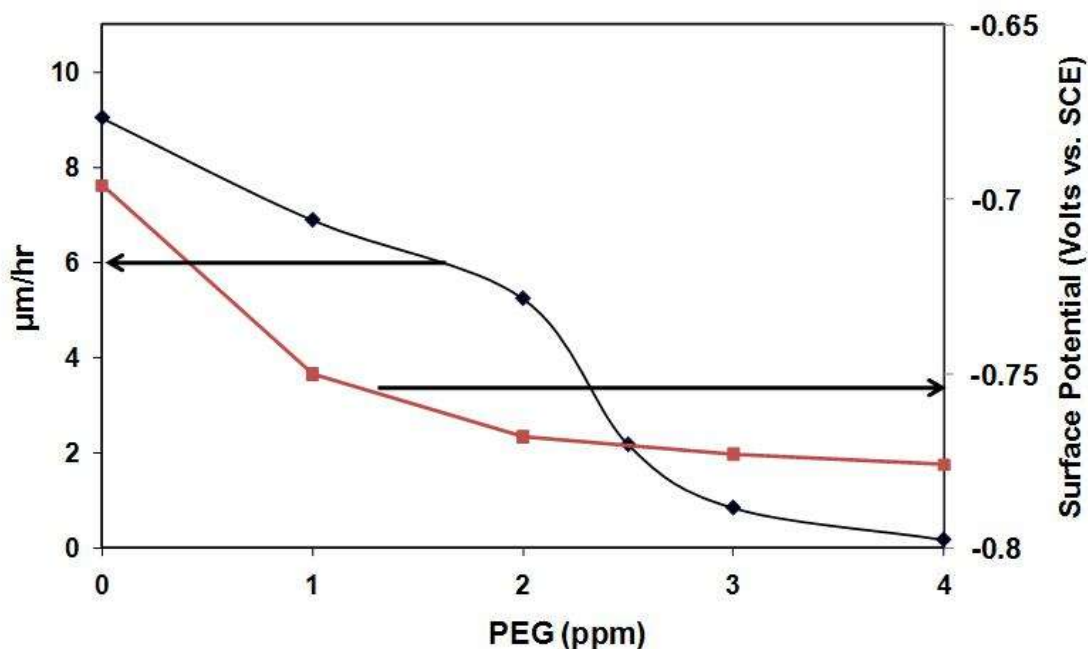


Figure 7.3: Deposition rate of the electroless bath as a function of PEG concentration and the surface potential versus SCE

In addition to being a plating rate inhibitor in electroless copper, PEG has been shown to be a leveling agent for acid copper electroplating. The leveling effects of PEG could be valuable in pillar-to-pillar plating to control the area of the pillar surfaces which may begin to grow at higher than desired rates. In narrow trenches and restricted spaces, the diffusion of PEG may be limited and lead to a deficiency which would result in higher deposition rates. For example, the deposition rate measured for 0 ppm PEG was 9.05 μm per hour, and the rate at 3 ppm PEG, was 0.85 μm per hour. This leveling effect could lead to a greater plating rate in restricted areas and the seamless pillar-to-pillar bonds.

Copper pillars were pre-fabricated on silicon substrates and flip-chip assembled, as previously discussed⁸. The test samples were electrolessly copper plated and joined using copper baths with different PEG concentrations. The samples were then potted in epoxy and cross-sectioned prior to any annealing to analyze the joint between the deposited metal. Figure 7.4 shows the results for samples plated with 1, 2, and 3 ppm PEG at 70°C.

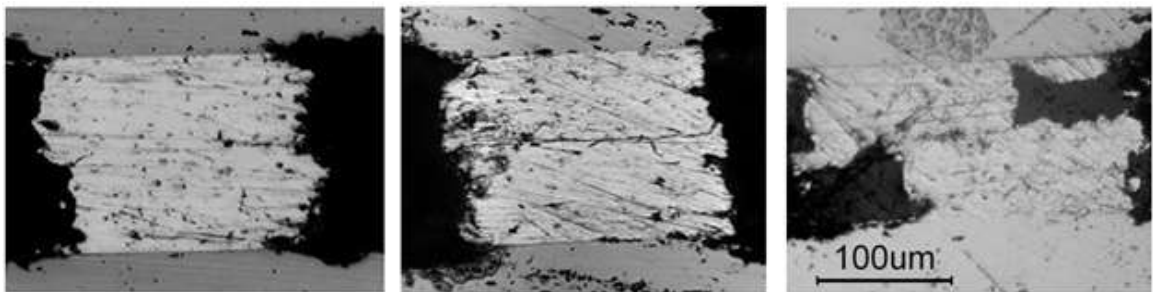


Figure 7.4: Cross-sections after electroless deposition and prior to annealing (left) 1 ppm PEG, 2 hours (middle) 2 ppm PEG, 3 hours, (right) 3 ppm PEG, 6 hours

Each sample was plated for a given time based on the separation between the pillars and deposition rates given above. The 1, 2, and 3 ppm PEG baths were plated for 2, 3, and 6 hours, respectively. The cross-section images show that the previously observed seam between the pillars is still present. However, all three samples showed no significant porosity or hydrogen bubble entrapment as was seen from the additive-free baths. The 1 ppm PEG deposition process filled the gap in 2 hours, which is a 9-fold reduction in plating time compared to the original room temperature additive-free process, which required 18 hours. This is a significant reduction in plating time and brings the pillar-to-pillar bonding process to a time scale more comparable to solder and underfill times.

The final step was to anneal the samples and create mechanically stable joints. Using an anneal temperature of 180°C for 1 hour in nitrogen ambient as reported previously [61], the joints recrystallized and formed mechanically stable, pillar-to-pillar bonds. Figure 7.5 shows two typical cross-sections for joints that were successfully bonded with the 180°C, 1 hour annealing process. The interface has been removed and has formed a seamless solid copper-copper bond. It is significant that the anneal process still allows for adequate recovery of the mechanical properties of the joint and the copper that was deposited to fill the gap between the copper pillars recrystallized sufficiently to provide mechanical strength.

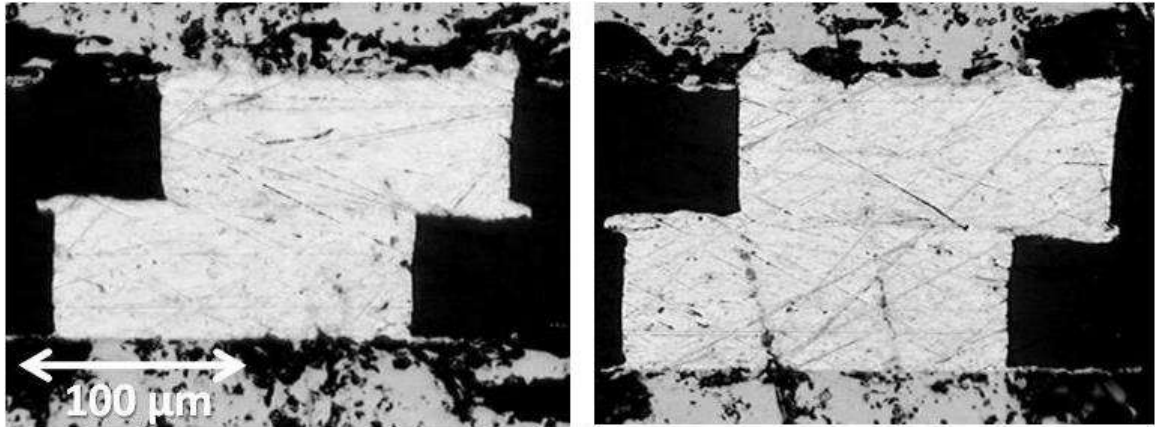


Figure 7.5: Cross-sections of two bonds plated with 1 ppm PEG for 2 hours after annealing at 180 C for 1 hour

In addition to cross-sections, mechanical shear tests were performed. The results for the samples plated with the 1 ppm PEG solution for 2 hours and then annealed at 180°C for 1 hour showed a shear force to break of 14.0 N. This force is directly comparable to results we have reported previously for shear tests with the same die using the previous, slow plating process. [60]

7.4 Discussion

The deposition and bonding process described here provides a significant reduction in the processing time for all-copper, flip-chip connections. The total time for plating and annealing for a 25 μm pillar-to-pillar gap was reduced from 19 hours to 3 hours, which includes one-hour anneal in each case. Further reductions in the plating time could be achieved by reducing the gap between the copper pillars from 25 μm to a narrower value. For example, if the planarity of the components could be improved, and the gap reduced to as small as 5 μm, the plating process would only require 24 minutes. To improve the deposition rate, the critical concept was to increase the temperature to

elevate both transport and kinetics, but then inhibit the deposition mechanism. In this case, the inhibition was provided by surface coverage of PEG. The net effect was to increase the plating rate from the previously described room temperature condition.[61] The inhibition allowed for transport of reactants and products onto and out of the seam between pillars so as to create solid, porosity-free copper deposits. Electrical contact between the copper pillars occurs prior to annealing, however, the strength of the bonded joint is not adequate until after annealing. A finer, more complete seam-filling plating process may reduce the need for annealing or lower its time and temperature. Further work on this will be pursued and may require additional additives to accelerate deposition in the seam during the last stages of plating.

7.5 Summary

The all-copper flip-chip plating process was improved by accelerating the plating process but keeping it under kinetically controlled deposition conditions. The inclusion of PEG in the electroless bath allowed a significant reduction in the time required to complete the bonding process, from 19 hours to 3 hours. The experiments showed that electrically joined bonds are formed during deposition and that mechanically reliable joints are formed by recrystallization and ‘knitting’ during annealing.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusion

The scope of this work was to develop a process that yields all-copper connections from the chip to the package substrate. The all-copper process must respect the needs for packaging in terms of cost and manufacturability. Typical packaging houses do not use cost prohibitive on-chip processing techniques such as any process requiring a vacuum (i.e. plasma deposition, plasma etching, sputtering). In addition the process must be competitive or better than solder in all areas that solder excels. These are primarily related to misalignment tolerance, and low temperature processing. Packaging with cost-effective organic printed circuit boards requires that elevated temperature excursions be as low as possible, but definitely below 250 C. The final goal of this work was to design copper pillar connections so as to be compliant and reliable without the need for underfill materials. This will eliminate the need for underfill materials and processing, possibly saving costs and at the same time increasing the possible I/O density without worry for underfill flow.

A novel process was developed to create solid copper-to-copper connections between the chip and substrate. Electroless copper deposition followed by low temperature annealing at 180 C for 1 hour created solid, mechanically sound copper joints. The bond strength was characterized as a function of anneal temperature and found that the mechanical strength of the copper joint exceeded the adhesion of the pillar to the chip. With an additional annealing step prior to bonding, to anchor the pillar to the

chip, the bond yield strength with a 180 C 1 hr anneal for the joint was found to be approximately 165 MPa. The electroless deposition showed large process dexterity with respect to planar and height mismatches between the two copper pillars. This capability will be key to maintaining low-cost processing, requiring lower tolerances on the flip-chip alignment. Bonding of copper pillars between Si and FR-4 was demonstrated and showed that the recrystallization and bonding process for the copper joining is maintained even under the CTE mismatch stress of the package.

The copper pillar and polymer collar system was modeled to minimize the stress that the pillar applies to the silicon chip surface. Since the industry is moving towards on-chip interconnect networks that require the use of brittle inter-metal dielectric materials to meet low-k requirements, stress on these networks in the package is a serious concern. It was found that the elastic modulus of the polymer collar had a significant impact on the stress applied to the chip by the pillar. In fact, by using a correctly optimized modulus, the stress anywhere in the pillar can be reduced by half using a single polymeric material for the collar. To further reduce the stress, it was found that bi-layer collar worked even better. Having a stiff short collar near the chip and substrate surfaces, followed by a tall high aspect ratio collar of a more easily patterned material reduced the maximum stress even further. Despite the optimization of the collar properties, to satisfy the industry recommended stress levels, related to the yield stress of lead-free solder, elliptical copper pillars were designed. The ellipse shape was found to significantly reduce the stress and improve thermo-mechanical performance for any given pillar cross-sectional area. With the optimized collar and an ellipse A/B ratio of 1.5, the stress target of 45 MPa was achieved. Experimental validation of the model was performed by

fabrication of three different collar materials. Each material was then characterized for its mechanical properties and then the pillars surrounded by each material were shear tested. The results confirmed the model prediction that a higher elastic modulus collar reduced the stress for a given pillar height and diameter. The results also indicated that the hardness, or brittle nature, of the polymer could also be a very important property in real systems that the model did not take into account.

Fundamental characterization of the bonding process was performed. It was shown that during the electroless deposition process, electrically conductive metallic bonds are formed between the surfaces. The resistance of the bonds was decreased by one order of magnitude following the 180 C for 1 hour annealing process. A large drop in the resistance supports the concept that the bonding is initiated from specific sites that are bonded. Then, copper surface diffusion and recrystallization serve to ‘knit’ the seam together and finish creating the solid copper-to-copper joint. Electroless plating and bonding was also performed using gold. Gold-gold bonds were formed between pillars by using electroless deposition followed by annealing. This proof-of-concept showed that the bonding is not unique either to the chemistry of the electroless copper bath or copper metallurgy.

An improved deposition process that dramatically reduced the time for plating was developed. Using an elevated deposition temperature of 70 C and PEG based surface kinetics suppression a kinetically controlled deposition was maintained. Without suppression of the deposition rate at higher temperature, porosity was generated and bonding was not achieved. With 1 ppm PEG in the bath, a deposition time of 2 hours was demonstrated and mechanically stable bonds were formed after annealing the

structures at 180 C for 1 hour in nitrogen ambient. Altogether the new deposition and annealing process reduced the total time for the bonding from 19 hours to 3 hours. Reducing the time is an important step towards manufacturability for this bonding process.

In summary, this work has led to the development and extensive characterization and optimization of the all-copper flip-chip process. This future alternative for solder connections shows significant promise for high performance semiconductor applications. With significant challenges related to I/O count, pitch, operating frequency, power supply, and reliability, solder will need to be replaced. The process was shown to have many competitive capabilities compared to solder with respect to misalignment and low temperature processing. Two of the major issues facing all-copper connections have also been addressed. First, reducing the stress placed on the chip from the copper pillar was achieved by correctly designing the polymer collar and geometry of the pillar itself. With elliptical connections, stress requirements for low-k on-chip networks can be met. Second, the dramatic reduction in process time utilizing the PEG based deposition bath makes the process more feasible for throughput requirements for manufacture. Making a reduction in process time from 19 hours to 3 hours, is a significant step towards manufacturability.

8.2 Future Directions for the All-Copper Process

The results for the all-copper process that were achieved in this work are significant. Yet, there are issues to address before the process can be considered a viable solder alternative for industry. First, thermo-mechanical reliability studies need to be performed. A sophisticated elastic-plastic model for the metal-polymer interconnect system should be used to predict thermal cycle reliability for the copper connections. Since this system differs greatly from the mechanical properties and concerns with solder, an in-depth study of the reliability affects is needed. Comparing these results to experimentally fabricated and thermally cycled samples will be critical to industry adoption. The second key aspect will be to test the limits of I/O pitch with this process. It is conceivable that the pitch will only limited by the lithography process to define the polymer collar molds. However, limitations may arise related to the electroless deposition. Neighboring pillars may plate into one another and cause electrical shorts. The effects of this on fabrication limits should be quantified to assess the roadmap for this process going forward. Finally, it would be desired to eliminate the deposition interface between the copper plating fronts. If seamless structures could be deposited without any need for an annealing step, reliable structures may be realized without need for temperature elevation. This would eliminate all the time and potential yield loss that will go into using the low temperature annealing step. Seamless through-hole plating has already been recently demonstrated [81] and should serve as a jumping off point for this work.

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